Logical Operations by Pulse Modulation in Nonlinear Directional Coupler

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***Abstract*— Implementation of logical gates by pulse modulation in nonlinear fiber directional coupler is investigated numerically. We consider pulses from an optical time-division multiplex system operating with pulse-position modulation (PPM). Such a system is simulated by a PPM modulator. The study shows that with a proper phase control it is possible to accomplish logical operations.**

***Keywords*— Pulse-position modulation, nonlinear directional coupler, soliton, logical gates.**

I. INTRODUCTION

Nonlinear directional coupler (NLDC) constructed from optical fiber is not a good candidate for obtainment of optical logic gates. The reason is the symmetric configuration does not support the obtainment of logic functions. In order to overcome this obstacle, we used the technique of pulse-position modulation (PPM), making two original proceedings: the use of a modulation and the result obtained. This fact itself represents an important contribution in the state of the art of the logic processing totally optical. Solving the nonlinear Schödinger equation (NLSE) numerically, it is possible to understand all the interaction process. For this analysis, it is considered, as an initial condition, the presence of two adjacent solitons, according to equation [1]:

$$\begin{aligned} A(0,T) \quad = \quad & A_{1e}\ sech\left[\frac{(T-T_r-T_{1e})}{T_0}\right] exp(i\phi_{1e}) + \\ & A_{2e}\ sech\left[\frac{(T-T_r-T_{2e})}{T_0}\right] exp(i\phi_{2e}), \quad (1) \end{aligned}$$

where A_{1e} and A_{2e} are the complex field amplitudes, ϕ_{1e} and ϕ_{2e} are the phases of each of the input fundamental solitons. T_{1e} and T_{2e} are the temporal displacement of the pulse peak in relation to the referential time T_r, where the initial time separation is given by $T_{1e} + T_{2e}$. When the solitons have different amplitudes, the behavior changes completely. For the case of solitons in phase ($\phi_{1e} = \phi_{2e}$), the collapse tends to disappear. For two out of phase solitons ($\phi_{1e} \neq \phi_{2e}$), which repelled before, repulsion tends to disappear [2].

In this work context, modulation is the process in which electronic digital data are converted to optical signals, which can be transmitted through optical fiber. The PPM, which is considered here, consists in the displacement of the original time position of the optical pulse by a low value of time τ. For temporal displacement with temporal increment ($+\tau$), the modulation represents the logical level 1 and for temporal displacement with time decrement ($-\tau$), the modulation represents the logical level 0. It is important to notice that the maximum temporal displacement of the modulated pulse should experience is $|\tau|$, otherwise, by definition, it will be considered as PPM error.

II. PROPOSED MODEL FOR NLDC LOGICAL GATES UNDER PPM MODULATION

Fig 1 shows our proposed model to investigate the performance of NLDC logical gates. We will consider that two optical solitons are incident on the inputs 1 and 2 located at $z = 0$. After they go through the PPM modulator, they are temporally displaced in relation to the referential time T_r according to the truth table of AND and OR logic gates ($T = T_r + \tau$ for bit 1 and $T = T_r - \tau$ for bit 0) [3]. Then, the phase control is applied in both pulses representing now the corresponding logic levels L_1 and L_2.

The achievement of AND and OR logic operations by NLDC is analyzed in each fiber or arm of the coupler

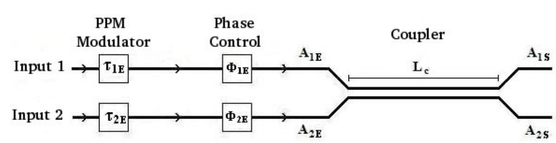


Fig. 1. Schematic diagram of a NLDC logical gate.

separately, observing that the maximum temporal displacement τ_s experienced by corresponding output pulse should be within the correct region limited to $-\tau \leq \tau_s < \tau$, with $\tau_s \neq 0$. The important thing is to yield a time displacement of the output pulses within the correct region for the adjustment parameter of the modulation for the whole system. The output pulse represents bit 1 when its time position is within the interval $0 < \tau s \leq \tau$ and bit 0 when $-\tau \leq \tau s < 0$ [4]. According to the truth table of AND and OR logic functions, for the combinations in which the input pulses represent different bits, i.e., $L_1 = 0$ and $L_2 = 1$ or $L_1 = 1$ and $L_2 = 0$, the output pulses should be within the interval $0 < \tau s \leq \tau$ (bit 1) to get OR logic operation, or within the interval $-\tau \leq \tau s < 0$ (bit 0) to get AND logic operation. For the two remaining combinations of the truth table, which correspond to equal bits, the interval in which τ_s should be found within the correct region is independent of the logic operation wished, AND or OR. For the case in which the input pulses represent the logic levels $L_1 = L_2 = 0$, the output pulses should always be within the interval for bit 0. Otherwise, when the input pulses represent the logic levels $L_1 = L_2 = 1$, the output pulses should always be within the interval for bit 1. The polarization effect is not the object of the present study, once it is initially relate to symmetry breaking problem. We cannot state yet if problems eventually related to polarization mode dispersion (PMD) or other factor related to polarization would assume an important role, taking the pulse width into account. Thus, this factor may be object of relevant study and research as a future perspective.

III. Simulation Theory and Numerical Procedure

The coupled partial differential equations describing the evolution of the slowly varying complex field amplitudes of the pulse envelope for the symmetric NLDC are:

$$\frac{\partial A_1}{\partial z} = i\kappa A_2 + i\gamma(|A_1|^2 + \sigma|A_2|^2)A_1 + -\frac{i}{2}\beta_2\frac{\partial^2 A_1}{\partial T^2} - \frac{\alpha}{2}A_1, \quad (2)$$

$$\frac{\partial A_2}{\partial z} = i\kappa A_1 + i\gamma(|A_2|^2 + \sigma|A_1|^2)A_2 + -\frac{i}{2}\beta_2\frac{\partial^2 A_2}{\partial T^2} - \frac{\alpha}{2}A_2, \quad (3)$$

where A_1 and A_2 are the amplitudes of initial solitons incident on the inputs 1 and 2 respectively (see Fig. (1), κ is the coupling coefficient among adjacent guides, α is the optic loss and the parameters γ, σ and β_2 represent the self phase modulation (SPM), cross phase modulation (XPM) and group velocity dispersion (GVD) effects, respectively, in each nucleus of the fiber coupler.

In this simulation, the input pulses have the full width at half maximum (FWHM) of $T_{FWHM} = 2.0\ ps$ and after the PPM modulation and phase control, its general form is given by:

$$A_{jE}(0,T) = \sqrt{P_0}\ sech\left[\frac{(T - T_r - T_d)}{T_0}\right]exp(i\phi_j) \quad (4)$$

where the index $j = 1, 2$ refers to input 1 or 2, ϕ_j is the inserted phase (control) and T_d is the temporal displacement, which represents the PPM adjustment parameter ($T_d = +\tau$ for bit 1 and $T_d = -\tau$ for bit 0) for the initial pulses. The temporal displacements of the input pulses are calculated in time position of maximum intensity, with $T_r = 0$ as reference time, corresponding to half of time slot.

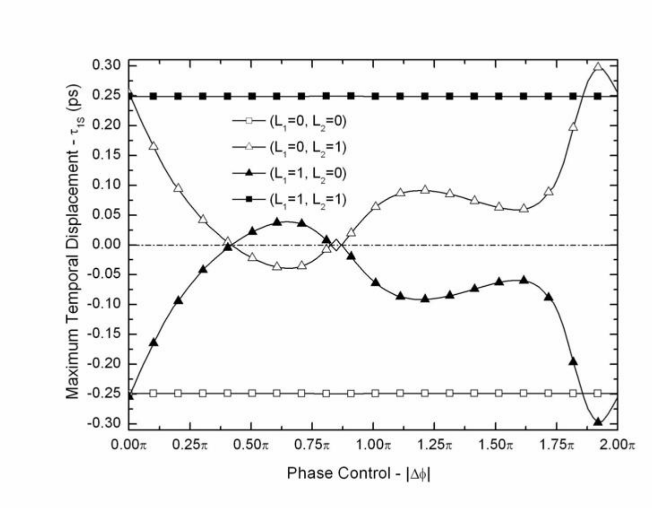
For our numerical analysis, L_j ($j = 1, 2$) represent the logical levels for the input pulses respectively, right after the PPM modulation. For the silica fiber operating in the wavelength region near 1.55 μm, the dispersion and nonlinearity coefficients are typically $\beta_2 = -20.0\ ps^2/km$ and $\gamma = 3.0\ W^{-1}/km$, respectively [2]. The input pulses fundamental solitons with pump power $P_0 = 5.18\ W$ which is required for the first order soliton propagation. It is assumed a coupling length $L_c = 64.30\ m$ and the coupling coefficient is $\kappa = 24.0\ km^{-1}$ .The critical power calculated is $P_C = 32.0\ W$ which is above the pump power P_0 [5].

The coupled partial differential equations Eqs. (2) and (3) was numerically solved using the 4th order Runge-Kutta method taking the initial conditions given by Eq. (4) into account, without loss ($\alpha = 0$). We also neglect the cross phase modulation effect ($\sigma = 0$).

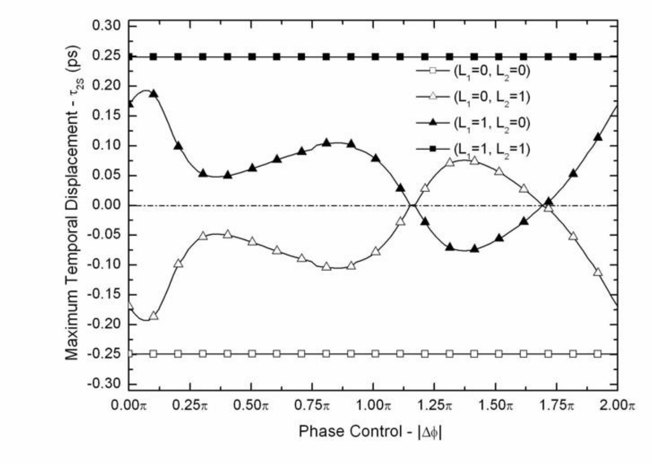
The analysis of the modulated soliton pulses is realized as describe in section II, i.e, a temporal displacement (τ) is applied to the input pulses and the maximum temporal displacement τ_{js} ($j = 1, 2$) of the correspondent output pulse is observed in relation to the same reference time T_r. Thus, the logic functions AND and OR are verified observing that the maximum temporal displacement of the output pulse can not exceed temporal displacements applied to the input pulses. In our simulation, we assign $\tau = 0.25\ ps$ what means that output pulses with temporal displacement between $0 < \tau_{js} \leq 0.25\ ps$ will play bit 1 and temporal displacement between $-0.25\ ps < \tau_{js} \leq 0\ ps$ will play bit 0.

IV. Results and Discussion

Fig. 2 shows temporal displacements as a function of $\Delta\phi$ between the input pulses when the phase is only applied to the pulse at the input 1 and Fig. 3 when the phase is only applied to the pulse at the input 2. The analysis shows that the phase difference variation of temporally overlapped input pulses does not modify the temporal position of output pulses in fibers 1 and 2, always remaining in the PPM error line. These pulses denote the cases ($L_1 = 0$, $L_2 = 0$) and ($L_1 = 1$, $L_2 = 1$), which always represent correctness for any applied phase difference. One can also notice that the behavior of the curves is symmetric around τ_{js} (dash-dot line in the Figs). Thus, there is not a $\Delta\phi$ such that the cases ($L_1 = 0$, $L_2 = 1$) and ($L_1 = 1$, $L_2 = 0$) occur inside of the same correct region for bit 0 or bit 1 and this fashion to obtain AND or OR logic gates. This means



(a)

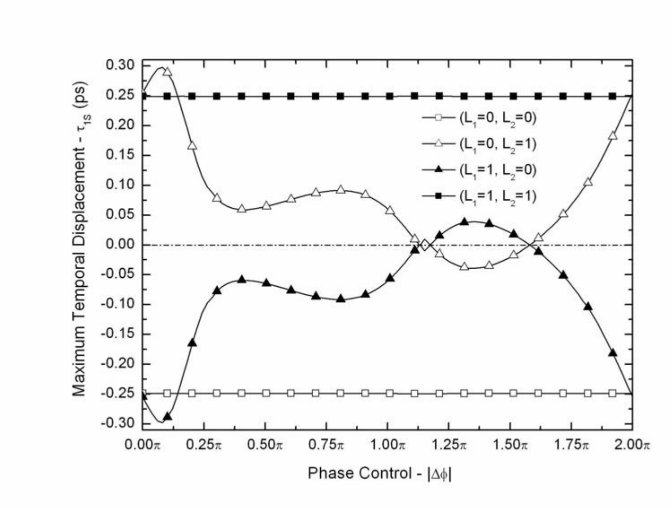


(b)

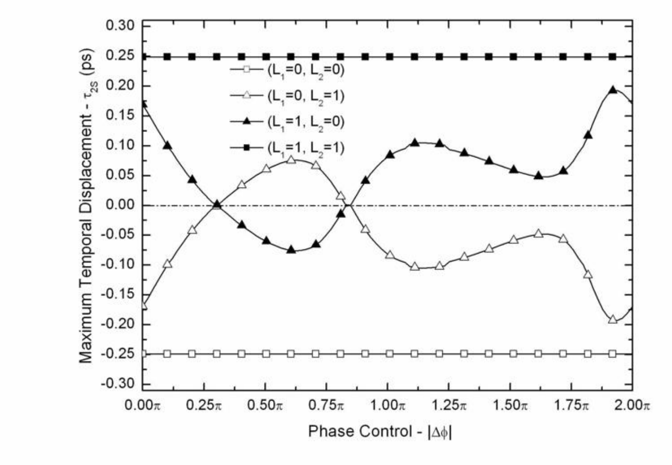
Fig. 2. Maximum temporal displacement as a function of $\Delta\phi$ between the input pulses with $\phi_2 = 0$. (a) for τ_{1s}, (b) for τ_{2s}.

that the achievement of AND or OR logic operations for the symmetric NLDC is not possible if the same phase is applied for the same input pulse in input 1 or 2, for four possible combinations of the truth tables. However, if it is decided to establish the phase control in agreement to each case of the truth table or logic levels of input pulses, the symmetric NLDC operation as logic gate becomes more complex, but, unlike before, it is possible to get AND and OR logic operations without PPM error. To accomplish this task, it was established the following logic rule to be performed by the phase control circuit: in the cases in which the pulse in fiber 1, right after the PPM modulator, has logic level 0, the phase should be applied to the pulse in fiber 2, otherwise, the phase should be applied to the pulse in fiber 1.

Fig. 4 shows the maximum temporal displacement as a



(a)

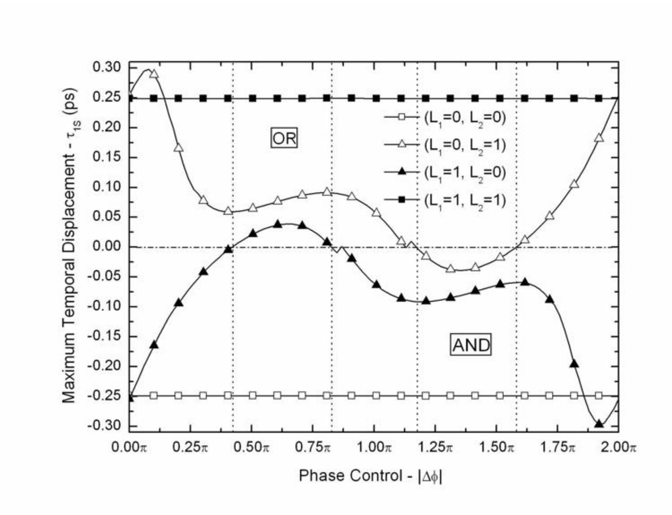


(b)

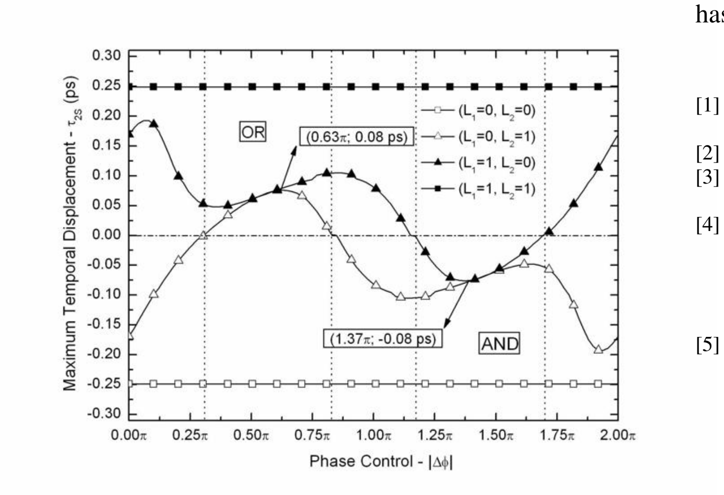
Fig. 3. Maximum temporal displacement as a function of $\Delta\phi$ between the input pulses with $\phi_1 = 0$. (a) for τ_{1s}, (b) for τ_{2s}.

function of $\Delta\phi$ between the input pulses for the cases ($L_1 = 0$, $L_2 = 0$) and ($L_1 = 0$, $L_2 = 1$) with $\phi_1 = 0$, and ($L_1 = 1$, $L_2 = 0$) and ($L_1 = 1$, $L_2 = 1$) with $\phi_2 = 0$. In Fig. 4(a), the results indicate that if the phase difference lays down in the interval $0.42\pi \leq \Delta\phi \leq 0.81\pi$ or $1.20\pi \leq \Delta\phi \leq 1.58\pi$, the cases ($L_1 = 0$, $L_2 = 1$) and ($L_1 = 1$, $L_2 = 0$) are shifted to the PPM correct region for bit 1 or bit 0, respectively. A similar result is observed in Fig. 4(b) but the phase difference must lay down in the interval $0.32\pi \leq \Delta\phi \leq 0.85\pi$ for bit 1 and $1.17\pi \leq \Delta\phi \leq 1.68\pi$ for bit 0.

It is important to notice that the extreme values of these phase intervals are very close to the boundary line or decision line $\tau_{js} = 0$ (logic level transience), what implies in greater probability of error in the achievement



(a)



(b)

Fig. 4. Maximum temporal displacement as a function of $\Delta\phi$ between the input pulses. $\phi_1 = 0$ when ($L_1 = 0$, $L_2 = 0$) or ($L_1 = 0$, $L_2 = 1$). $\phi_2 = 0$ when ($L_1 = 1$, $L_2 = 0$) or ($L_1 = 1$, $L_2 = 1$). (a) for τ_{1s}, (b) for τ_{2s}.

of the Boolean algebra for AND and OR logic functions. In this way, for a greater stability in the operation of the symmetric NLDC logic gate, it becomes necessary to use values of phase which guarantee a displacementτ_{js} the farthest possible from $\tau_{js} = 0$ for both cases ($L_1 = 0$, $L_2 = 1$) and ($L_1 = 1$, $L_2 = 0$).

V. Conclusion

The implementation of logic gates has been investigated numerically by using NLDC under PPM modulation in soliton regime. It was verified that if the same phase is applied in only one of the input pulses, it is not possible to achieve AND or OR logic operations because the cases ($L_1 = 0$, $L_2 = 1$) and ($L_1 = 1$, $L_2 = 0$) lay down in different correct region for bit 1 or 0. However, when the phase control is established in agreement with the logic level of the pulse in input 1, for each case of the truth table, what means to apply the rule in which if $L_1 = 0$ then $\phi_1 = 0$ or $L_1 = 1$ then $\phi_2 = 0$, the AND and OR logic gates were obtained when the phase difference lays down in the interval $0.42\pi \leq \Delta\phi \leq 0.81\pi$ and $1.20\pi \leq \Delta\phi \leq 1.58\pi$, respectively, for pulses emerging from output 1. A similar situation was verified for pulses emerging from output 2, but with phase difference into other interval.

Therefore, AND and OR logic operations based on symmetric NLDC can be accomplished without PPM error insertion, taking the values of $\Delta\phi$ and τ into account, for the stable operation of the logic gate.

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