

Impact of Bit-Channel Reliability Disparity on the Performance of LDPC Codes

Luíza M. de Freitas, Fernanda Smith, and Bartolomeu F. Uchôa-Filho

Abstract—This work investigates Low-Density Parity-Check (LDPC) codes in short block-length regimes, which are highly relevant for future communication systems. Although LDPC codes are known for their near-capacity performance, their efficiency can be limited when the code length is reduced, particularly in scenarios involving heterogeneous bit-channel reliabilities. Recently, Smith et al. have considered an LDPC coding technique to improve the error performance by exploiting the unequal bit-channel reliabilities. Reliability classes for variable nodes were defined, with constraints so the most reliable bits support the least reliable ones. The present study reveals that there is an optimum gap between these two extreme reliabilities that maximizes the performance gain. Initial simulation results showing this principle are presented, shedding light on short LDPC-Polar code concatenation.

Keywords—LDPC codes, low latency, short block length, unequal error protection, bit-channel reliability.

I. INTRODUCTION

Digital communication systems rely on efficient error-correcting codes to ensure reliable data transmission in the presence of noise and interference. Among the most prominent coding techniques, Low-Density Parity-Check (LDPC) [1] codes stand out due to their excellent performance and relatively low decoding complexity. Their sparse parity-check matrix structure enables the use of iterative decoding algorithms, such as belief propagation, which can achieve performance close to the Shannon limit [2].

LDPC codes have been widely adopted in modern communication standards, including wireless systems, satellite communications, and data transmission protocols. Their effectiveness is particularly evident in long block-length scenarios, where their asymptotic properties allow for highly reliable communication. However, in practical applications requiring short block lengths—such as low-latency communications and emerging real-time services [3]—their performance may degrade due to limitations in code structure and decoding convergence.

One important aspect often overlooked in conventional LDPC decoding is the assumption that all bit-channels experience identical reliability. In many practical scenarios, however, different bits may be transmitted under unequal conditions, leading to variations in their effective signal-to-noise ratios

(SNRs). Ignoring this heterogeneity can result in suboptimal decoding performance.

This observation has motivated previous research on incorporating unequal bit-channel reliability into LDPC-coded system design. In particular, the work in [4] investigated LDPC-coded QAM systems, where different bits of the modulation symbols inherently experience distinct levels of reliability. Orthogonal Frequency Division Multiplexing (OFDM) in frequency-selective fading channels were also considered, where different subcarriers undergo different fading gains.

The authors proposed a root-like bit mapping strategy, inspired by the root LDPC codes proposed by Boutros et al. [5] for the block-fading channel, combined with constraints on the parity-check matrix, to better match the code structure to the reliability profile of the bit-channels. The concept involves establishing reliability classes (good and bad) for variable nodes, and the constraints are designed so that the most reliable bits assist those with lower reliability. Using EXIT chart analysis, they demonstrated that properly exploiting this imbalance can improve the error performance.

Albeit these advances, to the best of the authors' knowledge, the impact of the bit-channel reliability disparity on these LDPC coded systems' performance has not been properly investigated. How does the method in [4] perform as a function of the SNR gap between the highest and the lowest bit-channel SNRs? Is there an optimal SNR gap under which the method produces the maximum performance gain? Conversely, for an existing channel scenario with a given SNR gap, can we design an LDPC coded system under the method in [4] that performs optimally under this gap? Also, how much the performance can be improved by modifying the channel log-likelihood ratios (LLRs) to reflect the different bit-channel reliabilities? Extending the study in [4], in this work, we try to answer all these questions. We show a simple demonstration of these ideas and present initial simulation results.

Specifically, we design and test a rate 60/120 LDPC code under different, artificially created bit-channel reliability gaps. This is done by varying the bit-channel SNRs in a controlled manner, while keeping the average SNR fixed. The design rules followed in [4] are realized by properly selecting some of the columns of the parity-check matrix to satisfy certain constraints, while the remaining columns are obtained with the Progressive Edge-Growth (PEG) algorithm [6]. Through Monte Carlo simulations, the LDPC coded system with binary phase-shift keying (BPSK) modulation is evaluated over the additive white Gaussian noise (AWGN) channel in terms of bit error rate (BER). The results demonstrate that combining reliability-aware modeling, PEG-based code construction, modified LLR computation, and appropriate bit permutation

L. M. de Freitas and B. F. Uchôa-Filho are with Department of Telecommunications, Division of Electronics Engineering, Aeronautics Institute of Technology (ITA), São José dos Campos, SP 12228-900, Brazil. E-mails: luiza.freitas.102091@ga.ita.br, bartolomeu@ita.br. F. Smith is with Department of Exact and Technological Sciences, Federal University of Amapá (UNIFAP), Macapá, AP 68903-419, Brazil. E-mail: fernandasmith@unifap.br. This work was partially supported by FAPESP (under grant no. 2025/01704-9), and by CNPq under grant 306623/2026-9.

leads to performance gains compared to classical LDPC-coded schemes with essentially no added decoding complexity.

The main motivation of the present study is to help shed light on the problem of concatenating short LDPC and Polar codes [7]. Virtual bit-channels with different qualities appear naturally in Polar coding. For short block-length, some intermediate bit-channels do not polarize, presenting varying qualities, which degrades the performance. Therefore, the study presented in this paper is of utmost importance to guide this code concatenation.

The remainder of this paper is organized as follows. Section II presents the preliminaries, including an overview of LDPC codes, the Sum-Product decoding algorithm, the PEG construction method, and the LLR definitions. Section III introduces the root-like LDPC code framework and the associated bit-mapping strategies designed to exploit unequal bit-channel reliabilities. Section IV presents the numerical results, evaluating the performance of the proposed approach over the AWGN channel. Section V discusses the future application of this study to the LDPC-Polar code concatenation problem. Finally, Section VI concludes the paper.

II. PRELIMINARIES

A. LDPC Codes

Low-Density Parity-Check (LDPC) codes are a class of linear block codes characterized by a sparse parity-check matrix, which enables efficient iterative decoding and excellent error-correction performance. Originally introduced by Gallager, these codes have gained widespread adoption in modern communication systems due to their ability to approach channel capacity with relatively low complexity.

An LDPC code is defined by a parity-check matrix $\mathbf{H}$ of dimension $(N - K) \times N$, where N is the codeword length and K is the number of information bits. The matrix $\mathbf{H}$ is sparse, meaning that it contains a small number of nonzero elements compared to its total size. Each valid codeword $\mathbf{c}$ must satisfy the parity constraint

$$\mathbf{H} \cdot \mathbf{c}^T = \mathbf{0}. \quad (1)$$

The sparse structure of $\mathbf{H}$ allows the representation of the code by a bipartite graph, known as a Tanner graph, composed of variable nodes (representing codeword bits) and check nodes (representing parity constraints). This graphical representation is fundamental for iterative decoding algorithms.

LDPC codes can be constructed either randomly or with algebraic structure. In this work, parity-check matrices are generated using the PEG algorithm [6], which incrementally builds the Tanner graph while avoiding short cycles. By maximizing the local girth and balancing node degrees, the PEG algorithm produces codes with improved decoding performance, particularly in finite-length regimes.

In addition to unstructured constructions, a widely used class of structured LDPC codes is the class of quasi-cyclic LDPC (QC-LDPC) codes. In QC-LDPC codes, the parity-check matrix is composed of circulant submatrices, allowing a compact representation through a smaller base matrix. This structure enables efficient hardware implementation, reduced

memory requirements, and simplified encoding using shift-register techniques. Despite their structured nature, properly designed QC-LDPC codes can achieve performance comparable to that of randomly constructed LDPC codes.

Decoding is performed using the Sum-Product Algorithm (SPA), also known as belief propagation. This iterative method operates on the Tanner graph by exchanging messages between variable and check nodes. These messages are typically expressed as LLRs, which quantify the reliability of each bit. One of these LLRs is the so called channel LLR, which reflects the bit channel quality and contributes to the total LLR of the bit. In conventional LDPC decoding, it is typically assumed that all bit-channels experience identical reliability, resulting in a uniform SNR, and therefore the same channel LLR, across all bits. However, this assumption does not hold in scenarios where different bits are transmitted under unequal conditions, which are usually known in advance (e.g., from achievable rates of bits in QAM or reliability sequences of Polar codes). Motivated by this observation, this work considers adjusting the channel LLRs across bits based on effective bit-channel SNRs.

This reliability-aware perspective is central to the proposed approach, as it allows the investigation of how structured variations in channel quality can be exploited to improve decoding performance, particularly in short block-length regimes.

B. PEG Algorithm

A modified version of the PEG algorithm is employed for the construction of the LDPC parity-check matrix. Unlike the conventional PEG approach, which initializes the matrix without any pre-existing structure, the proposed method incorporates a partially pre-designed matrix prior to the execution of the algorithm. This modification is motivated by the need to enforce specific structural constraints derived from the system model under investigation.

More specifically, the parity-check matrix $\mathbf{H}$ is partitioned into two distinct regions, such that

$$\mathbf{H} = [\mathbf{S} \ \mathbf{T}],$$

where $\mathbf{S}$ denotes the left submatrix and $\mathbf{T}$ denotes the right submatrix.

Submatrix $\mathbf{T}$ is designed beforehand according to the criteria established in Smith et al. [4], where a root-like structure is imposed to account for unequal bit-channel reliabilities in LDPC-coded QAM systems. In addition to the construction rules in Smith et al. [4], WIMAX-based restrictions are imposed as supplementary constraints. This ensures structural consistency and guarantees invertibility of the encoding representation while preserving the original root-like reliability mapping. This pre-designed submatrix ensures that the desired mapping between variable nodes and reliability classes (e.g., good and bad bit-channels) is preserved, thereby enforcing the conditions required for the analysis.

The left submatrix $\mathbf{S}$, on the other hand, is constructed using the PEG algorithm. However, instead of starting from an empty graph, the algorithm operates on the partially defined Tanner graph induced by the pre-designed right submatrix. Therefore,

the edge growth process must respect the existing connections while completing the remaining structure.

An example of the structured parity-check matrix obtained with the PEG construction is

$$\begin{bmatrix} 10 & -1 & -1 & -1 & -1 & -1 & 43 & -1 & -1 & -1 & -1 & \textcircled{15} & 0 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ -1 & 3 & -1 & -1 & 29 & -1 & -1 & -1 & -1 & 5 & -1 & -1 & 0 & 0 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ -1 & 1 & 6 & -1 & -1 & 17 & -1 & -1 & -1 & -1 & -1 & -1 & 0 & 0 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ 33 & -1 & -1 & -1 & -1 & -1 & -1 & 34 & -1 & -1 & 16 & -1 & -1 & -1 & 0 & 0 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ -1 & 32 & -1 & -1 & -1 & -1 & 35 & -1 & -1 & -1 & -1 & -1 & -1 & 0 & 0 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ -1 & -1 & -1 & -1 & -1 & -1 & -1 & 59 & -1 & -1 & 0 & -1 & -1 & -1 & 0 & 0 & -1 & -1 & -1 & -1 & -1 & -1 & -1 \\ -1 & -1 & 63 & -1 & -1 & -1 & -1 & -1 & 14 & -1 & -1 & -1 & -1 & -1 & -1 & 0 & 0 & -1 & -1 & -1 & -1 & -1 & -1 \\ -1 & -1 & -1 & 55 & -1 & -1 & -1 & -1 & -1 & 4 & -1 & -1 & -1 & -1 & -1 & -1 & 0 & 0 & -1 & -1 & -1 & -1 & -1 \\ 6 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & 29 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & 0 & 0 & -1 & -1 & -1 & -1 & -1 \\ -1 & -1 & -1 & -1 & 34 & -1 & -1 & 8 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & 0 & 0 & -1 & -1 & -1 \\ -1 & -1 & -1 & 55 & -1 & -1 & -1 & 56 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & 0 & 0 & -1 & -1 \\ -1 & -1 & -1 & -1 & -1 & 16 & -1 & -1 & -1 & -1 & 0 & \textcircled{15} & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & 0 \end{bmatrix} \quad (2)$$

In this representation, the circled entries correspond to one of the WIMAX conditions, that requires that the two circled values be identical, ensuring consistency in the imposed encoding structure. Furthermore, $\mathbf{S}$ is defined as the submatrix extending from the first column up to the column immediately preceding the circled element. The remaining columns compose the pre-designed submatrix $\mathbf{T}$.

The matrix in (2) is shaped as the compact representation of a Quasi-Cyclic Low-Density Parity-Check (QC-LDPC) parity-check matrix. Instead of explicitly storing the full binary matrix, each entry represents a $b \times b$ circulant submatrix, b being an expanding factor. In this notation, the value “−1” denotes an all-zero submatrix, while any non-negative integer represents a cyclically shifted identity matrix. For example, the entry “10” corresponds to an identity matrix with columns cyclically shifted by 10 positions, whereas “0” represents the standard identity matrix.

During the PEG construction, edges are progressively added between variable nodes and check nodes following the standard principle of maximizing the local girth. At each step, for a given variable node, a breadth-first search (BFS) tree is expanded over the current graph to identify candidate check nodes that maximize the shortest cycle length. Among these candidates, the check node with the lowest degree is selected to promote degree balance. Importantly, the search is constrained by the pre-existing edges, ensuring that no connections violate the imposed structure.

A key objective of this adapted PEG procedure is the elimination of short cycles, particularly cycles of length four (girth-4), which are known to significantly degrade the performance of iterative decoding algorithms. By combining the structured design of the right submatrix with the cycle-avoidance properties of PEG in the left submatrix, the resulting parity-check matrix achieves both compliance with the reliability-aware design constraints and improved graph properties, such as larger girth and better decoding performance. This hybrid design enables the integration of application-specific requirements—such as unequal error protection—while preserving the desirable characteristics of PEG-based LDPC codes.

C. LLRs

LLRs play a central role in LDPC decoding, as they provide a quantitative measure of the reliability of each coded bit. Instead of exchanging hard decisions, iterative decoding algorithms operate on soft information expressed in terms of probabilities.

For the coded bit $v_i \in \{0, 1\}$, assuming uniformly distributed source, the *a priori* probabilities are given by

$$p(v_i = 0) = p(v_i = 1) = \frac{1}{2}. \quad (3)$$

The corresponding *a priori* LLRs are defined as

$$L(v_i) = \log \left(\frac{p(v_i = 0)}{p(v_i = 1)} \right) = 0, \quad i = 1, \dots, N. \quad (4)$$

The *a posteriori* LLRs, given observation of the received vector $\mathbf{r}$, are given by

$$L(v_i|\mathbf{r}) = \log \left(\frac{p(v_i = 0 | \mathbf{r})}{p(v_i = 1 | \mathbf{r})} \right), \quad i = 1, \dots, N, \quad (5)$$

which include the channel information and takes into account the code structure. The Sum-Product decoding algorithm is an efficient way to obtain these *a posteriori* LLRs. The final decision on the coded bits is obtained from these LLRs.

After receiving the channel observation r_i , the Sum-Product decoder computes the i -th channel LLR as

$$L(v_i|r_i) = \log \left(\frac{p(v_i = 0 | r_i)}{p(v_i = 1 | r_i)} \right). \quad (6)$$

For transmission over an additive white Gaussian AWGN channel with BPSK modulation, this expression simplifies to a linear function of the received signal:

$$L_{c_i} = \log \left(\frac{P(v_i = 0 | r_i)}{P(v_i = 1 | r_i)} \right) = 4r_i \frac{E_s}{N_0}, \quad (7)$$

where r_i is the received signal corresponding to the transmitted bit v_i , and $E_b/N_0 = E_s/RN_0$ is the signal-to-noise ratio per bit.

In conventional LDPC decoding, all bits are typically assumed to experience identical channel conditions, resulting in uniform LLR statistics. However, as mentioned in Section II-A, in practical scenarios with unequal bit-channel reliability, different bits may exhibit distinct LLRs due to variations in their effective E_b/N_0 .

Motivated by this observation, this work adopts a reliability-aware LLR model, in which each bit is associated with a specific noise variance according to its assigned reliability class. By explicitly incorporating these variations into the LLR computation, the decoder can better distinguish between highly reliable and less reliable bits, improving the convergence behavior of the iterative decoding process, particularly in short block-length regimes.

III. ROOT-LIKE BIT-MAPPING

A promising approach to leverage unequal bit-channel reliability is the use of structured bit-mapping strategies. In particular, the root-like bit-mapping framework proposed in [4] introduces a mechanism where bits transmitted over highly reliable sub-channels assist those transmitted over less reliable ones. In this framework, the variable nodes of the Tanner graph are partitioned into three subsets, as illustrated in Fig. 1, according to the reliability of the sub-channels to which they are mapped:

- *Bad nodes*: associated with low-reliability sub-channels;

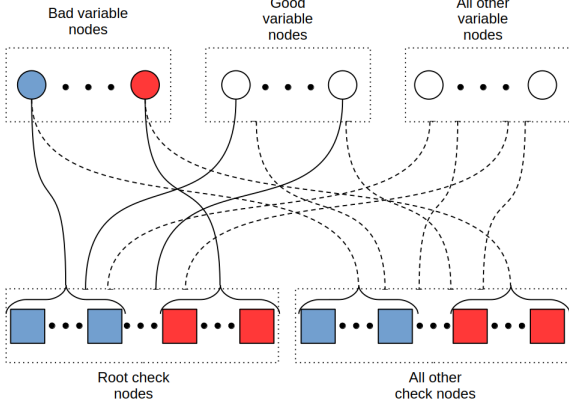


Fig. 1. Tanner graph for the root-like bit mapping scheme.

- *Good nodes*: associated with high-reliability sub-channels;
- *All other nodes*: without specific structural constraints.

The key idea is to enforce structural properties in the Tanner graph such that [4]:

- Bad nodes are not directly connected through short cycles;
- Each bad node is connected to at least one good node via a check node.

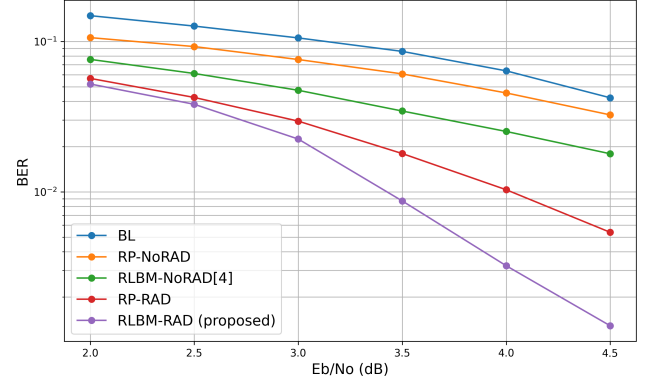
This structure enables reliable information from good channels to support less reliable bits during iterative decoding. The figure also highlights the presence of dedicated check nodes, referred to as *rootcheck* nodes, which are responsible for connecting good and bad variable nodes.

The graph in Fig. 1 was designed to promote reliable message propagation during iterative LDPC decoding. Preventing short cycles among bad nodes avoids the accumulation of unreliable LLR information in the same region of the graph, while connections to good nodes enable reliable information to assist the decoding of bits transmitted over poorer sub-channels.

Another important aspect visible in the Tanner graph is the distinction between mandatory and optional connections. The solid edges represent mandatory connections required by the root-like construction, whereas dashed edges correspond to optional connections that may be added according to the LDPC code design strategy. This organization preserves the sparse nature of the Tanner graph while enforcing the cooperation mechanism between reliable and unreliable variable nodes. As a result, the root-like bit-mapping structure improves decoding convergence and enhances the overall error-correction performance of the LDPC-coded system.

IV. EVALUATING THE IMPACT OF BIT-CHANNEL RELIABILITY DISPARITY: NUMERICAL RESULTS

This section presents numerical results assessing the performance of the proposed reliability-aware LDPC framework over an AWGN channel. The focus is on short block-length regimes, where conventional LDPC codes typically exhibit limited error-correction capability due to reduced code diversity and less effective iterative decoding.


 Fig. 2. BER performance versus (average) E_b/N_0 (dB) of the LDPC code with $N = 120$ and rate 0.5 represented by (2), under different configurations, for the SNR gap $\alpha = 15$ dB.

Simulations are carried out using the LDPC code with block length $N = 120$ and rate $R = \frac{1}{2}$, represented by the parity-check matrix in (2) with expanding factor $b = 5$. Decoding is performed using the SPA with the number of iterations fixed to 100. The performance metric adopted throughout this section is the BER as a function of E_b/N_0 .

To investigate the role of heterogeneous bit-channel reliability, a parameter α is introduced to artificially create a reliability gap across bit-channels. Specifically, a subset of channels is made more reliable by increasing their effective E_b/N_0 by $\alpha/2$ dB, while another subset is degraded by the same amount. The remaining channels retain the nominal value. This controlled imbalance allows evaluation of how reliability diversity can be exploited during decoding.

Fig. 2 shows the BER performance for $\alpha = 15$ dB under different configurations. We adopt the acronyms **RP** and **RLBM** for random bit permutation and root-like bit mapping, respectively. We also adopt the acronyms **RAD** for reliability-aware decoding, i.e., having the channel LLR adjusted at the bit level to the effective SNR, and **NoRAD** for uniform channel LLR based on the average SNR. Five scenarios are considered: **BL**: a baseline case without bit permutation and without reliability-aware decoding, **RP-NoRAD**, **RP-RAD**, **RLBM-NoRAD** from [4], and the proposed **RLBM-RAD**.

The results reveal several important trends. The baseline configuration consistently exhibits the worst performance, confirming that uniform treatment of bit-channels fails to exploit potential diversity. Random permutation provides only marginal gains, indicating that simple reordering without structure is insufficient.

In contrast, the structured permutation leads to noticeable improvements, even without modifying the decoding metrics (channel LLRs). However, the most significant gains are achieved when structured permutation is combined with reliability-aware log-likelihood ratio computation. In this case, the decoder fully exploits the unequal reliability of the channels, resulting in faster convergence and lower BER.

Fig. 3 presents the BER performance of the proposed

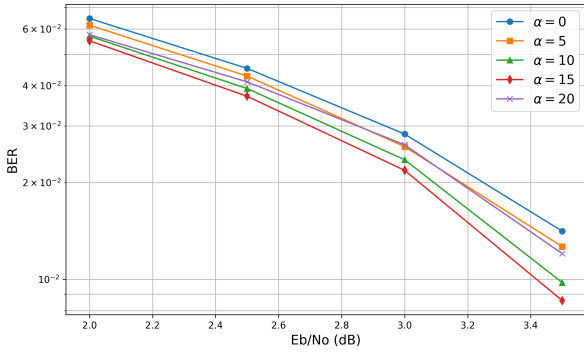


Fig. 3. BER performance versus (average) E_b/N_0 (dB) of the LDPC code with $N = 120$ and rate 0.5 represented by (2), under the proposed approach RLBM-RAD, for $\alpha = 0, 5, 10, 15$, and 20 dB

scheme for different values of α . An optimal or close to optimal performance is observed at $\alpha = 15$ dB. This is precisely the point at which the assistance of good bits to bad bits coming from the proposed approach is at its maximum. This behavior can be explained as follows. For small reliability gap, such as $\alpha = 5$ dB, bad bits are not that bad compared to good bits. Therefore, not much help is needed. Also, the good bits are not good enough to offer much help. Consequently, the performance improvement is small. On the other hand, if the reliability gap is very large, such as $\alpha = 20$ dB, not even ultra-reliable bits are able to compensate for the extremely poor performance of the bad bits, i.e., the decoding process operates beyond a breaking point.

From these results, we come to the conclusion that structured permutation aligns the code structure with channel conditions, ensuring that more important bits are transmitted over more reliable channels. Reliability-aware LLR computation enables the decoder to correctly interpret the varying confidence levels of received bits. Increasing reliability disparity improves decoding up to a certain point, beyond which the presence of highly unreliable channels begins to degrade the overall performance. These results indicate that deliberately introducing and exploiting heterogeneous bit-channel reliability can be an effective strategy for improving error-correction performance, particularly in short block-length regimes.

V. FUTURE WORK REGARDING 6G APPLICATIONS

The results obtained in this work are not only relevant in the context of standalone LDPC coding but also serve as a foundation for future developments. In particular, the proposed reliability-aware framework and bit permutation strategies are intended to be incorporated into a concatenated coding scheme involving LDPC and Polar codes. In such a scenario, the insights gained here will be used to enhance the protection of specific bit-channels, contributing to improved overall performance in short block-length communication systems.

This perspective is aligned with recent advances in coding techniques for 6G networks, driven by applications such as virtual and augmented reality, massive Internet of Things (IoT), and ultra-reliable low-latency communications. Polar

codes have emerged as strong candidates for these scenarios; however, their performance remains limited at short block lengths when used in isolation [3]. This limitation is fundamentally related to the polarization process, which does not produce a sharp separation between highly reliable and highly unreliable bit-channels, being a typical scenario where the proposed framework can be applied.

VI. CONCLUSIONS

This work investigated a reliability-aware LDPC code operating in short block-length regimes under heterogeneous bit-channel conditions. Unlike conventional LDPC coded systems, where all bits are assumed to experience identical channel reliability, the proposed approach explicitly incorporates unequal bit-channel qualities into both the code construction and decoding processes. Specifically, we adopted a PEG-based parity-check matrix construction—subject to certain structural properties in the Tanner graph—designed to allow reliable information from high-quality channels to support less reliable bits. Bit permutation strategies and modified LLR calculations were employed to better align the LDPC code structure with the underlying reliability profile of the transmission channels.

The main contribution of this work was the identification of an optimal reliability gap—between bad and good bit channels—that maximizes the error performance of the designed LDPC coded system. Simulation results over the AWGN channel demonstrated that the proposed reliability-aware strategies provide BER improvements compared to conventional LDPC code implementations, particularly when appropriate bit permutations and LLR adaptations are employed. The results also indicate that exploiting heterogeneous reliability conditions can improve decoding effectiveness in short block-length scenarios. The insights obtained from this work will be used, as future work, in the integration of the proposed methods into concatenated Polar-LDPC architectures and the evaluation of their performance in 6G-oriented communication scenarios.

REFERENCES

- [1] R. Gallager, "Low-density parity-check codes," *IEEE Transactions on Information Theory*, vol. 8, no. 1, pp. 21–28, Jan. 1962. [Online]. Available: <http://ieeexplore.ieee.org/document/1057683/>
- [2] S.-Y. Chung, G. Forney, T. Richardson, and R. Urbanke, "On the design of low-density parity-check codes within 0.0045 db of the shannon limit," *IEEE Communications Letters*, vol. 5, no. 2, pp. 58–60, 2001.
- [3] S. Miao, C. Kestel, L. Johannsen, M. Geiselhart, L. Schmalen, A. Balatsoukas-Stimming, G. Liva, N. Wehn, and S. Ten Brink, "Trends in Channel Coding for 6G," *Proceedings of the IEEE*, pp. 1–23, 2024. [Online]. Available: <https://ieeexplore.ieee.org/document/10571997/>
- [4] F. Smith, E. Pelaes, and B. F. Uchôa-Filho, "EXIT charts analysis of a root-like bit mapping for LDPC-coded QAM systems," *Digital Signal Processing*, vol. 70, pp. 39–48, Nov. 2017. [Online]. Available: <https://linkinghub.elsevier.com/retrieve/pii/S1051200417301690>
- [5] J. J. Boutros, A. Guillén i Fàbregas, E. Biglieri, and G. Zémor, "Low-density parity-check codes for nonergodic block-fading channels," *IEEE Transactions on Information Theory*, vol. 56, no. 9, pp. 4286–4300, 2010.
- [6] X.-Y. Hu, E. Eleftheriou, and D. Arnold, "Regular and irregular progressive edge-growth tanner graphs," *IEEE Transactions on Information Theory*, vol. 51, no. 1, pp. 386–398, 2005.
- [7] E. Arıkan, "Channel Polarization: A Method for Constructing Capacity-Achieving Codes for Symmetric Binary-Input Memoryless Channels," *IEEE Transactions on Information Theory*, vol. 55, no. 7, pp. 3051–3073, Jul. 2009. [Online]. Available: <https://ieeexplore.ieee.org/document/5075875/>