

Study of Nonlinearities in Converters for In-Band Full-Duplex Broadband PLC Systems

Matheus T. Perencio, Yan F. Coutinho, Moisés V. Ribeiro

Abstract—This study investigates the effects of nonlinearities in analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) in an in-band full-duplex broadband power line communication (BB-PLC) system employing a digitally controlled analog interference cancellation (DCAIC) architecture with a normalized least mean squares (NLMS) adaptive filter for channel estimation. Numerical results based on measured PLC channels show that the DCAIC architecture is less sensitive to converter impairments than digital interference cancellation (DIC). Nevertheless, the results also reveal that DCAIC is still unable to effectively suppress nonlinear distortions, indicating that nonlinearity mitigation remains a major challenge that must be addressed in the design of IBFD BB-PLC systems.

Keywords—echo cancellation, in-band full-duplex, nonlinear distortions, power line communication.

I. INTRODUCTION

Broadband PLC (BB-PLC) systems are considered cost-effective for indoor applications since they leverage existing electrical infrastructure for high-speed data communication [1]. Nevertheless, BB-PLC technology continues to face specific challenges [2], including signal attenuation due to cable loss, frequency-selective channels and severe impedance mismatches arising from load dynamics. Consequently, new approaches to enhance the efficiency and effectiveness of power line communication (PLC) systems have been proposed. One promising approach is the in-band full duplex (IBFD) communication [3], which allows simultaneous data transmission and reception within the same frequency band. However, successful implementation of this technique requires effective echo cancellation (EC) to mitigate the self-interference (SI) produced by the transmitter, which remains a significant challenge [4].

Previous studies have explored EC techniques utilizing least mean squares (LMS)-based adaptive filter (AF). The authors in [5] introduced a fully digital EC architecture, referred to as digital interference cancellation (DIC), which is constrained by the dynamic range (DR) of the analog-to-digital converter (ADC). Subsequently, the digitally controlled analog interference cancellation (DCAIC) architecture [6] addressed this limitation but required additional iterations to converge, making it less suitable for linear time-variant (LTV) channels.

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Further research [7], [8] showed that the recursive least squares (RLS) AF outperforms LMS in highly LTV scenarios, albeit with increased computational complexity.

While existing studies often address quantization effects, they frequently overlook nonlinear distortions introduced by the analog front-end (AFE) of converters. Furthermore, most research on nonlinearities concentrates on power amplifiers [9], [10], employing a common modeling approach based on the Volterra series expansion [11]. Despite its importance, the impact of converter nonlinearities in IBFD BB-PLC systems remains underexplored.

This study focuses on nonlinearities in the AFE of ADCs and digital-to-analog converters (DACs), with the objective of evaluating how their distortions, together with quantization, influence the performance of IBFD BB-PLC systems. Furthermore, the normalized least mean square (NLMS) AF is employed as it offers a favorable balance between convergence speed and computational complexity for estimating the SI channel in both the DCAIC and, subsequently, the DIC architectures for comparison. Through numerical simulation, the DCAIC architecture outperforms the DIC at mitigating quantization effects; however, neither of them are capable of dealing with the nonlinearities introduced by the converters, highlighting a significant challenge and encouraging the research of nonlinear solutions for IBFD BB-PLC systems.

Nomenclature: $\mathbb{E}\{\cdot\}$ and $(\cdot)^T$ denote the expectation and transpose operator, respectively, while $\star$ denotes the convolution operator. Moreover, given $u \in \mathbb{R}$, $\text{round}(u) = \lfloor u + 1/2 \rfloor$, if $u \geq 0$, or $\text{round}(u) = \lceil u - 1/2 \rceil$, if $u < 0$, in which $\lfloor u \rfloor = \max\{m \in \mathbb{Z} \mid m \leq u\}$ and $\lceil u \rceil = \min\{n \in \mathbb{Z} \mid n \geq u\}$.

II. SYSTEM MODEL

Fig. 1 shows a point-to-point IBFD BB-PLC system, using the DCAIC architecture [6], from the perspective of the near-end node. The opposite node is referred to as the far-end node. Both nodes operate within a coherence time that allows the PLC channel to be modeled as a linear time-invariant (LTI) system, with a channel impulse response (CIR) denoted by $h_{\text{PLC}}(t) \in \mathbb{R}$. The information-carrying signals transmitted by the near-end and far-end nodes, $x(t)$ and $x_{\text{SOI}}(t)$, respectively, are both band-limited to B and modeled as zero-mean wide-sense stationary (WSS) random processes. The received signal $y_{\text{R}}(t)$ is corrupted by additive noise, $w(t)$, modeled as a zero-mean WSS random process.

Regarding the hybrid coupler, it is assumed that the CIRs $h_{\text{P1} \rightarrow \text{P2}}(t)$ and $h_{\text{P2} \rightarrow \text{P3}}(t)$ are ideally modeled, $h_{\text{P2} \rightarrow \text{P1}}(t) = h_{\text{P3} \rightarrow \text{P2}}(t) = h_{\text{P3} \rightarrow \text{P1}}(t) = 0$, and $h_{\text{P1} \rightarrow \text{P3}}(t) = h_{\text{SI}}(t)$, with $h_{\text{SI}}(t)$ being the LTI SI CIR. Assuming perfect synchronization

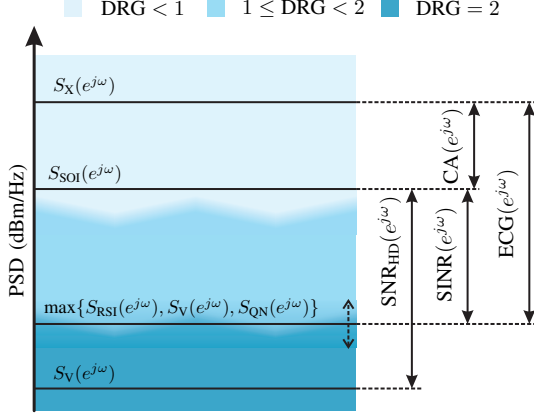


Fig. 2. Qualitative representation of the PSDs of the transmitted signals and noise obtained by the achieved ECG for a given ω . The shaded regions indicate the DRG.

nonlinearities — even though frequency-dependent memory effects typically occur in practical broadband scenarios — with the aim of highlighting the vulnerability of conventional EC architectures. Furthermore, their failure under a static model implies inevitable failure under more severe memory effects. This model and the uniform quantization are described in the following subsections.

A. Memoryless Polynomial Model

Time-invariant nonlinear systems can generally be described using the Volterra series [11], which allows modeling of nonlinear systems with arbitrary memory, including dynamic effects dependent on multiple delays. However, parametric complexity grows exponentially with the order and memory [10]. To simplify the analysis, memoryless polynomial models¹ can be derived to represent nonlinear effects. Using this model, the relationship between the input $s[n]$ and the output $r_{NL}[n]$ of a DAC/ADC is modeled by [11]

$$r_{NL}[n] = \sum_{p=1}^P a_p s^p[n], \quad (7)$$

where $a_p \in \mathbb{R}$. As modern differential converters exhibit antisymmetry in the transfer curve around the origin, the coefficients associated with even powers become negligible compared to the odd terms [12]. In a moderate nonlinearity regime, the cubic term is primarily responsible for generating relevant harmonics and intermodulation products, resulting in

$$r_{NL}[n] = a_1 s[n] + a_3 s^3[n], \quad (8)$$

in which a_1 and a_3 can be obtained from the total harmonic distortion (THD) specifications of the converter as follows. Consider a sinusoidal input sequence given by

$$s[n] = A \cos(\omega_0 n). \quad (9)$$

¹A memoryless polynomial model is obtained from the Volterra series when only the zero-delay kernel coefficients are retained and all memory terms are discarded.

Now, apply the memoryless cubic model, then the intermediate analog output becomes

$$\begin{aligned} r_{NL}[n] &= a_1 A \cos(\omega_0 n) + a_3 A^3 \cos^3(\omega_0 n) \\ &= \left(a_1 A + \frac{3}{4} a_3 A^3 \right) \cos(\omega_0 n) + \frac{1}{4} a_3 A^3 \cos(3\omega_0 n). \end{aligned} \quad (10)$$

In a weak nonlinearity regime, the cubic contribution to the fundamental component is small compared to the linear term. Thus, the ratio between the amplitude of the third harmonic and the fundamental amplitude provides a direct approximation for the dominant THD, leading to the relationship

$$\text{THD} \approx \frac{\left| \frac{1}{4} a_3 A^3 \right|}{|a_1 A|} = \frac{|a_3| A^2}{4 |a_1|}. \quad (11)$$

Isolating the cubic coefficient, we obtain

$$a_3 \approx \frac{4a_1}{A^2} \text{THD}, \quad (12)$$

where the THD value must be used in a linear scale and the amplitude A must correspond to the excitation level employed in the converters' THD measurement.

B. Quantization Model

Considering the use of a symmetric uniform quantizer with b bits, the quantization step is expressed by

$$\Delta = \frac{2A}{2^b}. \quad (13)$$

Since the quantizer is symmetric around the origin, the number of positive levels is given by

$$K = 2^{b-1} - 1 \quad (14)$$

and the largest representable value before saturation is $A = K\Delta$, while the effective limit of the quantization region is given by $T = A + \frac{\Delta}{2}$. Assuming that the quantization is uniform mid-tread, i.e., it has a zero level, the converter output $r_q[n]$ is expressed by

$$\begin{aligned} r_q[n] &= \mathcal{Q}(r_{NL}[n]) \\ &= \begin{cases} A, & r_{NL}[n] \geq T, \\ \Delta \times \text{round}\left(\frac{r_{NL}[n]}{\Delta}\right), & \text{otherwise}, \\ -A, & r_{NL}[n] \leq -T, \end{cases} \end{aligned} \quad (15)$$

where $\mathcal{Q}(\cdot)$ is the quantization function. This construction leads to a model aligned with the structural properties of the converters. The composition of the polynomial with the quantization operator allows for the simultaneous capture of nonlinear distortions and finite resolution effects, providing a basis closer to practical IBFD BB-PLC systems.

IV. NUMERICAL RESULTS

This section evaluates the IBFD BB-PLC system based on the DCAIC [6] architecture. Furthermore, a comparison to the DIC [5] architecture is presented, considering three DAC/ADC models: an infinite precision model, a quantization-only model, which is denoted by $r_q[n] = \mathcal{Q}(s[n])$, and a joint nonlinear and quantization model as in (15).

As shown in Fig. 3, the channel frequency responses (CFRs) for both SI and PLC channels were obtained from a measurement campaign conducted in seven residences in the city of Juiz de Fora, which followed the methodology discussed in [13], wherein $L_f = L_{h_{SI}} = L_{h_{PLC}} = 200$. The PLC channel exhibits high CA compared to the SI channel. Also, we consider that the system is impaired by additive white Gaussian noise (AWGN) with $S_V(e^{j\omega}) = -130$ dBm/Hz, agreeing with the PLC noise PSD reported in the literature [14].

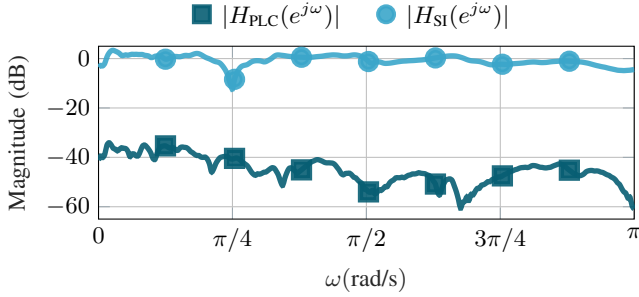


Fig. 3. CFRs of PLC channel and of the SI channel.

The transmitted signals were generated based on the hermitian symmetric orthogonal frequency division multiplexing (HS-OFDM) technique with a 4-QAM constellation, bandwidth $B = 100$ MHz, $N = 2048$ subcarriers in this frequency range, and a cyclic prefix length $L_{CP} = 512$. The sampling frequency used was $f_s = 200$ MHz, which results in a symbol period $T_{sym} = (2N + L_{CP})/f_s = 23.04$ μ s. The PSD of the transmitted signals was $S_X(e^{j\omega}) = -50$ dBm/Hz.

To match the quantizer's DR, we consider the normalization $\tilde{x}[n] = x[n] / (k \sigma_x)$ at the input of the converters, such that $A = 1$, in which σ_x is the standard deviation of $x[n]$ and $k \in \mathbb{R} \mid k > 0$ is the input back-off. We set $k = 5$ in our simulations to minimize the distortion caused by saturation on the system's performance [15]. We evaluate specific commercial ADCs with $b = \{8, 12, 16\}$ [16], [17], [18], and a DAC with $b = 16$ bits [19], selected since they operate within the frequency band of interest with low variation of THD range. Table I presents typical THD for these converters in nominal operating conditions for input frequency $f_{IN} \leq 100$ MHz, as well as the average THD and the respective a_3 coefficients obtained using (12), assuming $a_1 = 1$.

The performance is analyzed in terms of convergence rate and ECG obtained after AF convergence. The convergence rate is evaluated through the stochastic approximation of the mean squared error (MSE), which is given by

$$\text{MSE}[n] = \mathbb{E} \{e^2[n]\}. \quad (16)$$

The chosen AF was the NLMS [20], with a step-size of $\mu = 0.15$. The numerical results, obtained from 4,000 Monte Carlo realizations, are shown in Fig. 4 as $\text{MSE} \times \text{HS-OFDM}$ symbol and $\text{ECG}(e^{j\omega})$ for $b = b_{DAC} = 16$ bits for the DAC and $b = b_{ADC} \in \{8, 12, 16\}$ bits for the ADCs.

Regarding MSE, both architectures with infinite precision converge identically to the noise floor. In DCAIC architecture, the MSE is equal to the infinite precision one regardless

TABLE I
TYPICAL AND AVERAGE THD WHEN $f_{IN} \leq 100$ MHz FOR THE CONSIDERED CONVERTERS, AND RESPECTIVE a_3 DERIVED VIA (12).

	b	f_{IN} [MHz]	Typical THD [dB]	Average THD [dB]	a_3
ADC	8	4	-60	-57.40	5.396×10^{-3}
		20	-58		
		50	-60		
		70	-56		
		100	-53		
	12	5	-81	-77.67	5.231×10^{-4}
		30	-78		
		90	-74		
	16	10	-98	-93.25	8.701×10^{-5}
		30	-94		
		70	-93		
		100	-88		
DAC	16	20	-78	-74.33	7.684×10^{-4}
		50	-74		
		70	-71		

of b_{ADC} for the quantization-only model, but degrades significantly under the polynomial model, showing that this architecture is capable of mitigating quantization effects, but is not effective in suppressing nonlinear distortions. On the other hand, in the DIC architecture, the ADC DR is the main performance bottleneck. Although increasing b_{ADC} to 16 bits minimizes quantization noise, the polynomial model reveals that nonlinearities still prevent the MSE from reaching the noise floor.

In terms of ECG, when considering infinite precision, the maximum theoretical ECG for both architectures is achieved. The DCAIC architecture mitigates quantization effects, matching the infinite-precision case, but remains equally susceptible to nonlinear distortions. On the other hand, the achievable ECG in the DIC architecture increases with b_{ADC} . While the quantization-only model reaches the maximum ECG with a 16 bit ADC, the polynomial model does not, confirming that even 16 bits are insufficient under nonlinear effects.

Overall, the DCAIC architecture outperforms the DIC one. However, neither architecture effectively suppresses nonlinear distortions, highlighting the need for further research on techniques capable of mitigating nonlinearities in IBFD BB-PLC systems.

V. CONCLUSIONS

This paper analyzes the impact of nonlinearities and quantization effects on DACs and ADCs in IBFD BB-PLC systems. To do so, a third-order polynomial model with coefficients derived from typical THD values of commercial converters was employed. Numerical simulations were performed using the NLMS AF combined with the DCAIC architecture. The results show that, although well-established architectures can effectively mitigate quantization effects, they remain highly vulnerable to nonlinear distortions. Overall, the findings indicate that nonlinear distortion mitigation remains an open challenge in IBFD BB-PLC systems, motivating further investiga-

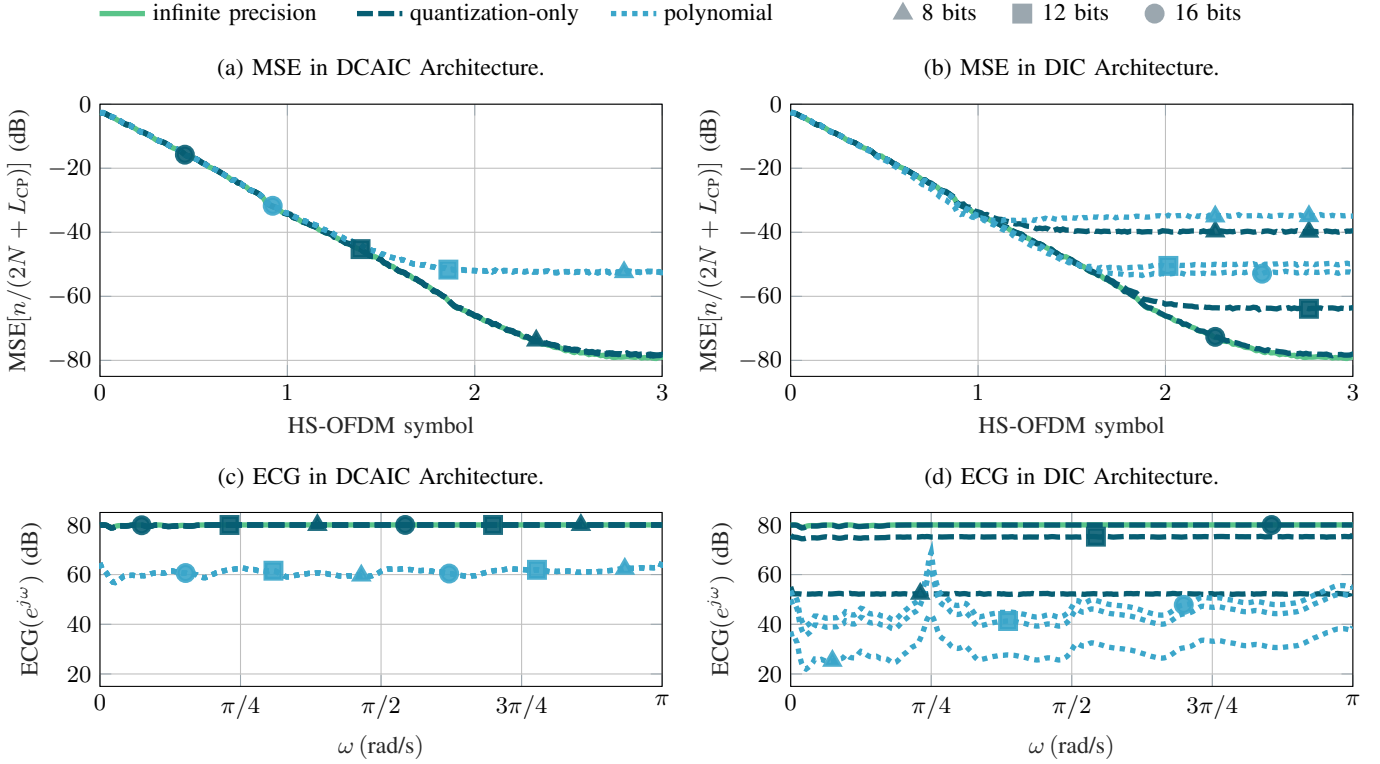


Fig. 4. MSE $\times$ HS-OFDM symbol and $ECG(e^{j\omega})$ for $b_{DAC} = 16$ bits and $b_{ADC} \in \{8, 12, 16\}$ bits in DCAIC and DIC architectures.

tion of techniques capable of jointly addressing quantization and nonlinear effects, such as the application of nonlinear AFs (e.g., Volterra-based algorithms) or neural cancellers.

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