

High-Frequency Protection for RF Front-Ends Under Severe Electromagnetic Disturbances

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Abstract—This paper presents a high-frequency protection mechanism designed to safeguard RF communication systems exposed to high-intensity electromagnetic anomalies. The proposed solution employs a dual-stage architecture that combines a fast-response clamping circuit with an active isolation stage based on a high-frequency relay. The first stage limits instantaneous overvoltage peaks, preventing the saturation and potential damage of sensitive front-end components. If the disturbance persists, the second stage disconnects the RF path and diverts excess energy to a dedicated dissipation network, ensuring continuous system integrity. Experimental results demonstrated that the architecture provides effective suppression of transient and sustained electromagnetic events while maintaining low insertion loss during normal operation. The proposed mechanism offers a robust and scalable protection strategy for demanding RF environments, with potential applications in communication, sensing, and mission-critical electronic systems.

Keywords—RF front-end protection, High-frequency circuits, Electromagnetic disturbances, Electromagnetic pulse immunity, Clipping circuits, RF isolation, High-frequency relay switching, Transient suppression.

I. INTRODUCTION

In radio communications, RF front-ends are inherently vulnerable to high-intensity electromagnetic disturbances, particularly in environments where strong electromagnetic emissions are expected. Such disturbances can couple into antennas and transmission lines, generating voltage and current surges that may exceed the safe operating limits of sensitive components. In this paper, the RF front-end denotes the interface between the antenna and the radio device. On the receive path, from the antenna port up to the first frequency-conversion stage, and on the transmit path, from the up-converter through the Power Amplifier (PA) to the antenna. It comprises matching and filtering networks, RF switches/duplexers, Low-Noise Amplification (LNA), local oscillator and mixer. This usage follows common practice in receiver/transceiver design and modern Radio Communication systems. [1] The literature consistently highlights that LNAs, mixers, and other RF front-end blocks are among the most susceptible elements to high-power or fast-rise RF pulses [2]. Moreover, complex electronic subsystems such as SoC (Silicon on chip) controllers, digital displays, and mixed-signal circuits may also suffer degradation or failure when subjected to strong electromagnetic interference [2].

Conventional front-end protection strategies rely on components such as PIN-diode limiters, gas discharge tubes (GDTs), Transient-Voltage Suppressors (TVS), and ferrite-based absorbers. PIN-diode limiters are widely used as it can reflect or dissipate large incident RF energy through a controlled

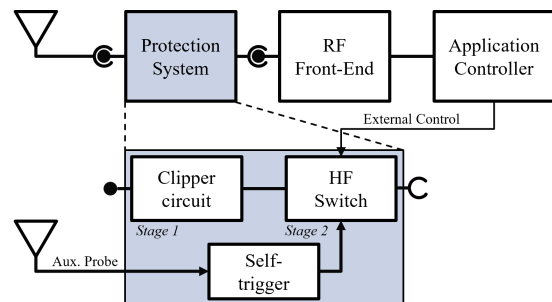


Fig. 1. Proposed dual-stage high-frequency protection architecture designed to safeguard RF front-ends under severe electromagnetic disturbances.

reduction in their effective RF resistance under high-signal conditions [3], [4], [5]. However, these circuits may struggle with short rise-time pulses and can increase significant insertion loss at high frequencies [3]. GDTs, while effective for high-energy surges, exhibit slow turn-on behavior and require high breakdown voltages, limiting their effectiveness for short-duration RF transients [6]. TVS devices provide fast response, but also a relatively high parasitic capacitance can compromise broadband RF performance, particularly in low-noise or high-frequency receive paths [6].

This work proposes a dual-stage high-frequency protection architecture designed to safeguard RF front-ends under severe electromagnetic disturbances, as seen in Fig.1. The *Stage 1* is a high-frequency clipping circuit based on PIN-diode limiting principles, capable of suppressing fast transients and preventing immediate overload of downstream components [6]. The *Stage 2* employs an active high-frequency relay that disconnects the RF path when persistent or high-energy anomalies are detected, diverting the excess energy to a controlled dissipation network. Combined, the both stages provide complementary protection: the clipping stage manages short-duration high-amplitude surges, while the relay stage ensures isolation during longer-lasting or cumulative electromagnetic events.

Furthermore, the proposed configuration allows the relay to actuate without external power by harvesting energy from the electromagnetic disturbance. Thus, the architecture has virtually zero power consumption: in idle, the *NC* contact keeps the link transparent; when activated, the disturbance itself provides the energy to drive the relay, which is advantageous for RF systems with tight battery-life budgets.

II. RELATED WORKS

Protection of RF front-ends against high-intensity electromagnetic disturbances has been widely studied, especially for electromagnetic pulse (EMP) immunity. Prior works propose mitigation of fast, high-power transients at RF receivers, *e.g.* in [7] the authors evaluate EMP-induced stress and compares semiconductor vs. gas-discharge strategies, while GaAs-Schottky limiters provide fast-response protection [8]; additional robustness under high-power jamming appears in [9], tailored to autodyne sensing systems. Advanced techniques for strong or repeated EMP events include semiconductor/switching-based strategies [10] and slow-wave delay structures for earlier action against fast-rising fronts [11]. Broadband SCR-triggered ESD (Electrostatic discharge) clamps further show the feasibility of fast HF clamping despite parasitic-capacitance limits [12]; device-level integration also appears in T/R switches with embedded ESD self-protection [13] and multifunctional ESD/power-limiting circuits for UHF RFID with minimal RF sensitivity loss [14].

Active isolation is a key approach for persistent electromagnetic stress. RF-MEMS (microelectromechanical systems) switches can deliver high isolation with improved hot-switching reliability [15], while mechanical RF relays handle substantial RF power [16]. These paths are complementary, and insights from wideband isolation in full duplex radio systems help guide broadband protection design [17]. Supporting literature on front-end architecture and device behavior highlights practical constraints that shape protection requirements [18], [19]. In parallel, low-capacitance ESD techniques in CMOS emphasize the core trade-off between device robustness and RF transparency [20]. Overall, prior work advances EMP protection, limiter circuits, ESD-tolerant structures, and isolation switching. Yet no single approach simultaneously provides fast clipping for short transients and active isolation for persistent overloads with minimal RF penalty in normal operation. This gap motivates the dual-stage high-frequency protection system proposed in this paper.

III. METHODOLOGY

The proposed protection system is conceived to operate in RF environments subject to severe electromagnetic stress while preserving the RF front-end receiving and transmitting performances.

A. Design Objectives and Constraints

The primary objectives are: (i) fast suppression of short-duration, high-amplitude transients; (ii) safe handling or redirection of persistent or high-energy incidents; (iii) minimal insertion/return loss during nominal operation; (iv) zero (or near-zero) standby power; and (v) low implementation complexity and cost. The architecture therefore combines two complementary layers: a passive, two-stage PIN-diode clipper at the RF input (*Stage 1*), and an actively isolated, relay-based diversion to dissipate overload energy to a matched 50Ω load (*Stage 2*). Both layers are designed to be self-activating by leveraging the energy available at the input, thereby eliminating the need for continuous biasing or external power sources.

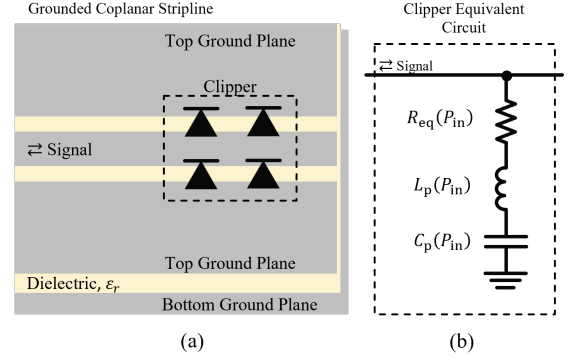


Fig. 2. Clipper stage with pair of high-frequency PIN diodes in anti-parallel at the RF input node. Two identical clipper stages are cascaded.

B. Overview of the Protection Architecture in Two Stage

The Fig. 1 consists of an RF input port, a cascaded two-stage limiter based on anti-parallel PIN diodes (*Stage 1*), the receiver path is routed through the normally closed contact of a high-frequency relay, and a shunt branch toward a 50Ω dissipative load (*Stage 2*). Under nominal signals, the limiter remains effectively transparent (low dynamic conduction, low parasitics), the relay remains closed, and the receiver experiences the nominal link. Under severe excitation, *Stage 1* clamps instantaneous peaks; if the incident power persists beyond the clipper's safe energy handling, *Stage 2* opens the receiver path and diverts energy to the matched load. The *Stage 2* actuation is self-triggered by a high-frequency rectifier that derives DC from the incident RF envelope, or by the application controller when available.

C. Stage 1: RF Clipper

The first protection stage consists of two pairs of high-frequency PIN diodes arranged in an anti-parallel, symmetric configuration at the RF input (Fig. 2(a)). This symmetry clips both positive and negative signal excursions and helps preserve wideband behavior [3]. The clipper can be represented by the power-dependent equivalent network in Fig. 2(b), where the effective resistance $R_{eq}(P_{in})$ and the parasitic reactances $L_p(P_{in})$ and $C_p(P_{in})$ vary with the incident power P_{in} due to charge injection and storage in the diode's *I*-layer under large-signal drive [3], [6].

For nominal inputs, R_{eq} remains high and the parasitic capacitance $C_p(P_{in})$ stays low, ensuring minimal passband insertion loss and acceptable return loss across the intended bandwidth [3]. In this condition, the clipper behaves nearly transparent to the radio application. As shown in Table I, in this work the resulting device have the insertion loss lower than 1.8 dB, and return loss below -19.71 dB.

As incident power P_{in} increases, carrier injection in the *I*-layer drives the diodes into a low conduction resistance, thus reducing $R_{eq}(P_{in})$ and clamping the peak voltage at the receiver port [3]. At the same time, the stored charge changes the reactive components so that $C_p(P_{in})$ increases and the effective inductance $L_p(P_{in})$ becomes smaller over the frequencies of interest, causing the limiter to exhibit a more

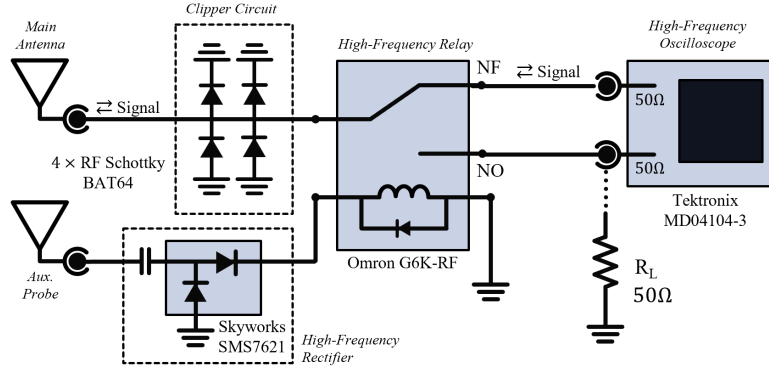


Fig. 3. Overall system concept detailing measurement setup and main components connections. The dissipative load (R_L), is not connect for this evaluation, as it only represents the final concept of the device.

reactive and lossy response under high-power conditions [3], [6]. The net effect is twofold: (i) higher dissipation, reflected as increased instantaneous insertion loss, and (ii) increased reflection due to the power-dependent mismatch created by the reactive shift. The both mechanisms contributing to limiting waveform excursions that would otherwise reach sensitive front-end components [3], [6].

Two identical clipper stages are cascaded to increase the overall *power-handling capability* without introducing distinct turn-on thresholds. In this case it was employed two BAT64 PIN diodes on each clipping stage [5]. Classical multi-stage clippers often combine PIN diodes with different I -layer thicknesses to stagger their conduction thresholds (a “coarse” limiter followed by a “clean-up” limiter), distributing energy across stages and suppressing residual spikes [6]. In contrast, to simplify the design and improve scalability, we use two stages with identical devices. Although this removes the intentional threshold differentiation, cascading identical stages still enhances energy retention before any residual leakage can reach sensitive front-end circuitry [6].

D. Stage 2: Self-Trigger Relay-Based Active Isolation

The post-clipper RF signal proceeds to the *normally closed* (NC) contact of a high-frequency relay (Omron G6K-RF), which keeps the receive path transparent under nominal conditions. When the self-trigger circuit detects high levels of incident energy, the relay opens the receiving path, diverting the input to a matched $50\ \Omega$ dissipative load (R_L in Fig. 3). Thus, the harmful energy is absorbed away from sensitive front-end components.

To avoid external power or continuous biasing, a high-frequency rectifier monitors the electromagnetic environment through an auxiliary probe, as seen in Fig. 3. When a strong EMP event occurs, the rectifier converts part of the incident RF energy into a DC voltage V_{act} proportional to the disturbance amplitude. Once $V_{act} \geq V_{relay}$, the relay driver energizes the coil and transitions the system into the protected state. This energy-harvesting mechanism ensures that a fraction of the harmful energy is repurposed to activate the protection circuitry, eliminating the need for dedicated bias

power. Optionally, when energy constraints are not a concern, the application controller may override or assist the trigger upon detecting abnormal RF exposure.

Both stages are passive or quiescent in standby, and does not demand any energy from the main application. The clipper requires no bias; its static loss is determined solely by small-signal parasitics. The relay remains de-energized in the NC state, and the high frequency rectifier chain is off until a sufficient envelope is present. Consequently, the architecture is suitable for low-power or power-constrained deployments where external energy sources are limited or intermittently unavailable.

IV. IMPLEMENTATION AND EXPERIMENTAL VALIDATION

For nominal input levels, the protection system was characterized using a Keysight PNA-L N5230C VNA. The adopted port map was: Port 2 = RF input; Port 1 = RF front-end path; and Port 3 = matched $50\ \Omega$ dissipative load (Fig. 3). Accordingly, S_{21} represents transmission toward the RF front-end, S_{22} the input return loss, and S_{23} the transmission toward the dissipative branch. As summarized in Table I, the nominal state exhibits low insertion loss toward the RF

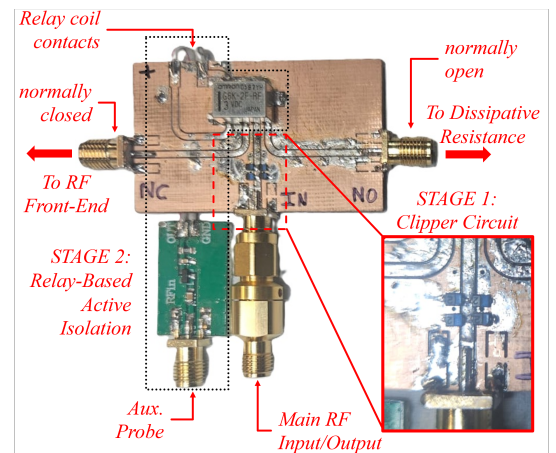


Fig. 4. Photographic register of the prototype in measurement setup.

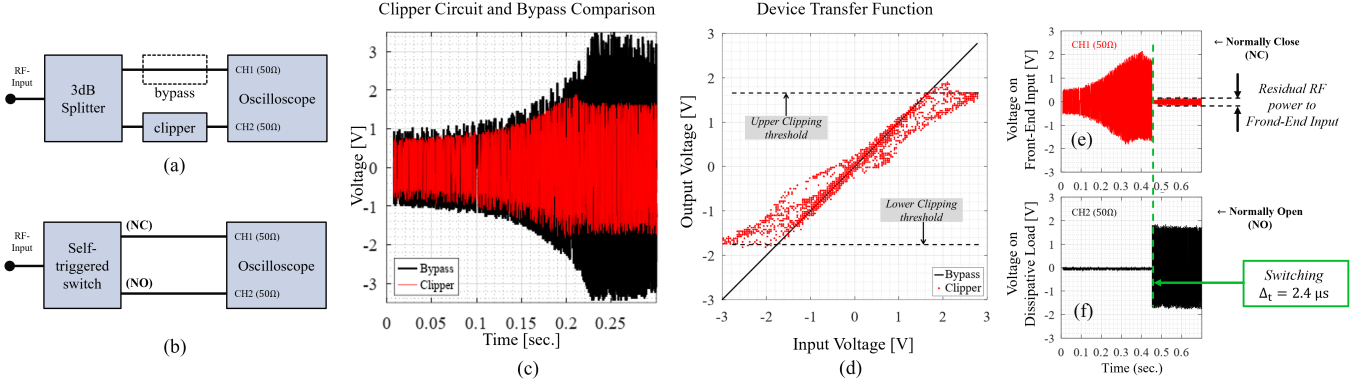


Fig. 5. Experimental validation of the dual-stage protection. (a) Setup utilized for evaluating clipper circuit results. (b) Setup utilized for Self-triggered switch evaluation. (c) Output amplitude (red) when the input envelope (black) increases. (d) The transfer function highlights the lower/upper clipping thresholds. (e–f) With the relay engaged, energy is redirected away from the RF front-end and into the dissipative branch. All oscilloscope inputs were terminated in 50 Ω.

front-end and low coupling to the dissipative load, while the protection state reverses this behavior, confirming the intended energy-diversion mechanism. Measurements under relay activation or limiter clipping require power levels beyond the safe operating range of the VNA, as the input power must not exceed 27 dBm [21]. Therefore, large-signal conditions were evaluated in the time domain using a high-speed oscilloscope. The adopted high-power RF oscillator does not reproduce standardized EMP waveforms and was used solely as a controlled source of electromagnetic stress for proof-of-concept validation of the clipping, isolation, and energy-diversion mechanisms. Validation under standardized EMC immunity test procedures is proposed for future work.

A. Time-Domain Validation and Power Estimates

All time-domain measurements were performed with the oscilloscope inputs terminated in 50 Ω to provide a well-defined load and minimize reflections under high-power excitation. Under these conditions, the clipper stage limited the measured waveform to approximately $V_p \approx 3.2$ V. For comparison, the same drive without the clipper produced $V_p > 10$ V at the measurement port.

Fig. 4 shows the time-domain influence of the RF clipper when the input envelope ramps up: the bypassed trace increases proportionally to the drive, whereas the clipped trace saturates near a fixed peak level. The corresponding transfer function in Fig. 4(d), that presents a linear regime around the origin that transitions to saturation beyond the lower/upper switching thresholds, making the limiting behavior visually

evident. Panels (c) and (d) document the relay-assisted protection: at the switching instant, the receiver-side node (CH1) collapses to a low residual level while the dissipative branch (CH2, 50 Ω) receives the diverted waveform, confirming the intended energy redirection, as seen in Fig.5(e) and Fig.5(f).

Assuming a sinusoidal waveform and a 50 Ω termination, the rms voltage and power are given by

$$V_{\text{rms}} = \frac{V_p}{\sqrt{2}}, \quad (1)$$

in which, $V_p = 1.5$ V, as seen in Fig. 4. Thus,

$$V_{\text{rms,clip}} = \frac{1.5}{\sqrt{2}} \approx 1.061 \text{ V}, \quad (2)$$

Hence, the power retained by clipper circuit is given, by:

$$P = \frac{V_{\text{rms}}^2}{50}. \quad (3)$$

Thus, for **clipping** case, it yields,

$$P_{\text{clip}} = \frac{V_{\text{rms,clip}}^2}{50} \approx 22.5 \text{ mW} (\approx 13.5 \text{ dBm}). \quad (4)$$

For the **no-clip** case, it was taken the peak input voltage from the *Stage 1* output (black plot in Fig. 4(c)) to evaluate the power diverted to the dissipative load. Taking the maximum value obtained during the tests to $|V_p| = 3.2$ V, in (1), it yields a maximum diverted power, given by:

$$P_{\text{no-clip}} \geq \frac{(3.2/\sqrt{2})^2}{50} \approx 102.4 \text{ mW} (\approx 20.1 \text{ dBm}). \quad (5)$$

Therefore, at the time-domain observation point the limiter provides at least 6 dB of power mitigation (peak excursion

TABLE I
S-PARAMETER COMPARISON UNDER NOMINAL AND PROTECTION (DIVERTED) CONDITIONS.

Condition	S_{21} (input→ RF) [dB]	S_{22} (input return) [dB]	S_{23} (input→ Load) [dB]
Protection State	−23.40	−10.61	−1.79
Nominal State	−1.50	−11.56	−19.71

Port-map: Port 2 = RF input; Port 1 = NC output (receiver path); Port 3 = dissipative load 50 Ω. Representative values measured at $f = 2.4$ GHz.

constrained from $3.2 V_p$ down to $1.5 V_p$). After the relay was actuated (protection state), the node corresponding to the RF front-end input exhibited a residual excursion of approximately $V_p \approx 100 \text{ mV}$, as seen in Fig. 4(e). As the oscilloscope still terminated in 50Ω , this yields:

$$V_{\text{rms,post-switch}} = \frac{0.10}{\sqrt{2}} \approx 0.0707 \text{ V}, \quad (6)$$

thus, residual power P_r delivered to the RF front-end, is

$$P_r = \frac{0.0707^2}{50} \approx 0.1 \text{ mW} (\approx -10 \text{ dBm}). \quad (7)$$

Combining the observed $\approx 6 \text{ dB}$ limiter attenuation with the additional isolation provided by the relay-diverted state ($\approx 20 \text{ dB}$, frequency-dependent), the system achieves an aggregate protection margin of approximately 26 dB . The complete switching time was measured as $\sim 2.4 \mu\text{s}$. Time-domain measurements at the 50Ω observation port indicate an effective clipping level of approximately 25 mW ($\approx 14 \text{ dBm}$), remaining transparent to typical low-power communication systems operating below 20 dBm . The adopted high-power RF oscillator does not reproduce standardized EMP waveforms and was used solely as a controlled source of electromagnetic stress for proof-of-concept validation of the clipping, isolation, and energy-diversion mechanisms. Validation under standardized EMC immunity test methodologies is left for future work.

V. CONCLUSIONS

We presented a high-frequency protection architecture for RF front-ends operating under severe electromagnetic disturbances. Measurements have confirmed that the prototype is capable of suppressing fast transients with minimal pass-band penalty, and perform a relay-based active isolation, redirects persistent or high-energy events to a matched dissipative branch. The device was successful in harvesting energy from the self electromagnetic disturbance to activate the relay based isolation. Frequency-domain measurements confirmed low loss in the nominal state, less than 1.8 dB . Overall, the combined clipper and relay behavior yielded an aggregate protection margin greater than 26 dB .

Future work should focus on adaptive trigger thresholds and hysteresis for multi-band operation, as well as solid-state or MEMS-based isolation to reduce switching latency. To support long-term product scalability, thermal modeling, redundancy in critical systems, and accelerated life testing under repeated pulse exposure will be conducted to enhance reliability.

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