A Compact 1:4 Power Divider for mmWave applications

Isaac G. Y. Rabello, Gustavo P. Rehder, Ariana Maria L. C. Serrano and Heitor Albuquerque

***Abstract*— This paper presents the design and simulation of a compact 1:4 power divider operating in 60 GHz based on the Webb divider. The device uses microstrip lines and 3D interdigitated capacitors on the porous alumina membrane, called MnM substrate. This design proposes to reduce the size of the lines of a conventional Wilkinson divider by 50%, resulting in a total size of 1.08 mm², insertion loss < 1 dB, isolation > 11 dB and a BW of 11 GHz (18.3%), and appears to be innovative in published materials in the area.**

***Keywords*— Power Divider, Compact, MnM substrate, 3D interdigitated capacitors.**

I. Introduction

The research on Millimeter-Wave devices is valuable and on the rise, as the need for data links with higher throughputs increases, and demands for military/defense technologies such as radars are growing. The miniaturization of circuits for the use in these extremely-high frequencies presents several challenges to designers due to semiconductor and process limitations.

Power dividers are one of the most classical passive circuits and its applicability may be seen in a myriad of devices. Being bi-directional, a divider can also be used as a combiner [4].

As an example, with the emergence of 6G technologies, such devices may be used to split a signal in order to feed multiple LPAs (Low Power Amplifiers), and then used to recombine and feed a single antenna with high power.

The default Wilkinson Power Divider [9] (WPD) is a robust and well tested design, but its solution yields lines of length $\frac{\lambda}{4}$, which might be considered too long for mmWave applications.

There are many solutions to N-port single-stage power dividers, but at some point the result becomes difficult to realize in a planar circuit due to the high impedances involved, resulting in very narrow lines, sometimes impossible to implement. This presents a challenge to the realization of such devices on cheap PCB (Printed Circuit Board) technology, as more layers are required to synthesize the layout. In higher frequencies, the use of more layers implies administering numerous unwanted effects that arise from the interaction (induction) between layers. A common alternative is to cascade various 2-port power dividers in order to get the needed factor.

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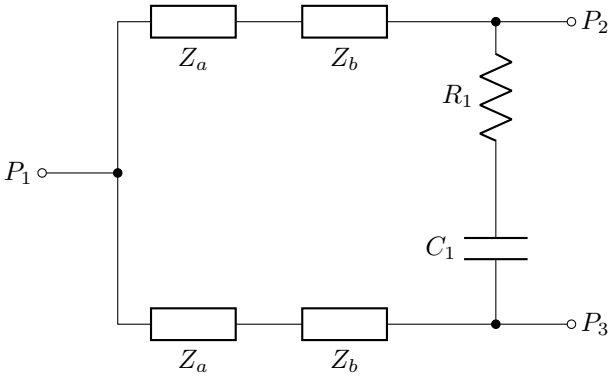

Fig. 1. 2-port Webb divider schematic

This paper presents a compact power divider (based on the Webb power divider) for higher frequencies, with lines of length $\frac{\lambda}{8}$, while maintaining acceptable isolation between ports. The proposed design cascades two 2-port dividers in order to get a 4-port divider at 60 GHz on inexpensive PCB technology.

II. Model and Schematic Simulation

The design proposed by Richard C. Webb [8] for a power divider is shown in Figure 1, where Z_x is the characteristic impedance of the line and P_n are the ports. The other parameters can be calculated with:

$$Z_a = \frac{Z_0}{\tan(\theta)}\sqrt{\sqrt{1+8\tan^4(\theta)}-1} \tag{1}$$

$$Z_b = \frac{2Z_0}{Z_a} \tag{2}$$

$$R_1 = \frac{(Z_a+Z_b)^2}{Z_0}\sin^2(\theta)\cos^2(\theta) \tag{3}$$

$$C_1 = \frac{1000}{2\pi f_{GHz}} \cdot 2\Bigg[(Z_a+Z_b)\sin(\theta)\cos^3(\theta) - Z_b\left(1+\frac{Z_b}{Z_a}\right)\sin^3(\theta)\cos(\theta)\Bigg]^{-1} (pF) \tag{4}$$

Where θ is the line electrical length.

In the Webb layout, two sections of unequal impedance are put in series, and a capacitor is added in series with the resistor in between the ports to compensate this inequality and improve port isolation. Notice that when $\theta = \frac{\lambda}{8}$, $Z_a = Z_b$, $R_1 = \sqrt{2}Z_0$ and the total length is $\frac{\lambda}{4}$, which is the same solution given by a regular WPD.

As the goal is a 50% reduction in line length, the parameters were calculated for $\theta = \frac{\lambda}{16}$. Promising S-parameter simulation results on *Keysight ADS*[7] for ideal components and conditions are shown in Figure 2. Consider for all layouts in this paper port 1 as input and ports 2 - 5 as output. The return loss in all ports (S(x,x)) is better than 54.8 dB in all cases. The insertion loss between the input and each output (S(h,1) where h ranges from 2 to 5) is better than 0.021 dB. And the isolation between output ports (2 - 5) is better than 51.6 dB.

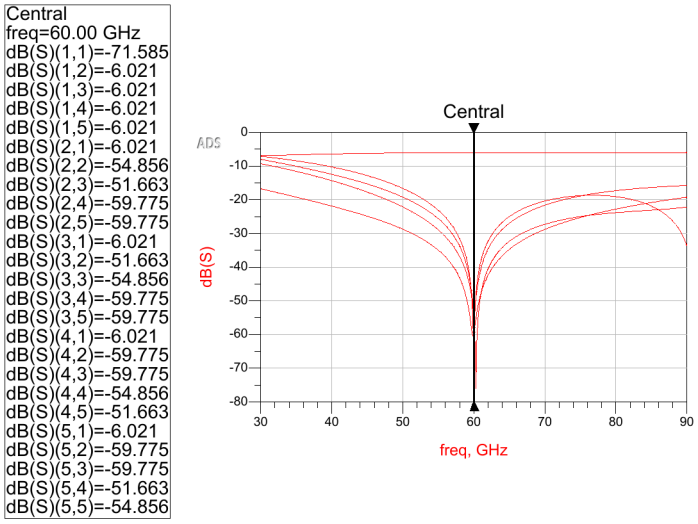

Fig. 2. S-parameter simulation for an ideal 1:4 Webb Power Divider @ 60GHz

When analyzed and optimized for an *RT/duroid® 5880* [5] ($\epsilon_r = 2.2$) substrate with *ADS LineCalc*, line dimensions were unattainable, as the line width was larger than line length. Using the MnM [6] (Metallic Nanowire-Filled Membrane) ($\epsilon_r = 6.7$) substrate, the circuit seemed realizable and resulted parameters after optimization $\left(\theta = \frac{\lambda}{16}\right)$:

- $Z_a = 40.3\Omega$ (0.1 mm x 0.14 mm)
- $Z_b = 124\Omega$ (0.006 mm x 0.15 mm)
- $R_1 = 67.5\Omega$
- $C_1 = 60fF$

A comparison between the substrates is shown in Table II

TABLE I
COMPARISON BETWEEN RT/DUROID® 5880 AND MNM SUBSTRATES

	RT/duroid® 5880 [1]	MnM
ϵ_r	2.2	6.7
H	$180\mu m$	$50\mu m$
$\tan(\delta)$	0.0009	0.01
T	$17.5\mu m$	$3\mu m$

The simulations for an "ideal layout" in the MnM substrate yielded the S-parameters shown in Figure 3. The return loss in all ports (S(x,x)) is better than 21.4 dB in all cases. The insertion loss between the input and each output (S(h,1) where h ranges from 2 to 5) is better than 0.133 dB. And the isolation between output ports (2 - 5) is better than 27.3 dB

[1]These values correspond to an RT/duroid® 5880 available at the lab. One may ask the vendor for another version of the substrate with slightly different values. However, none of the modifications possible would solve our problem.

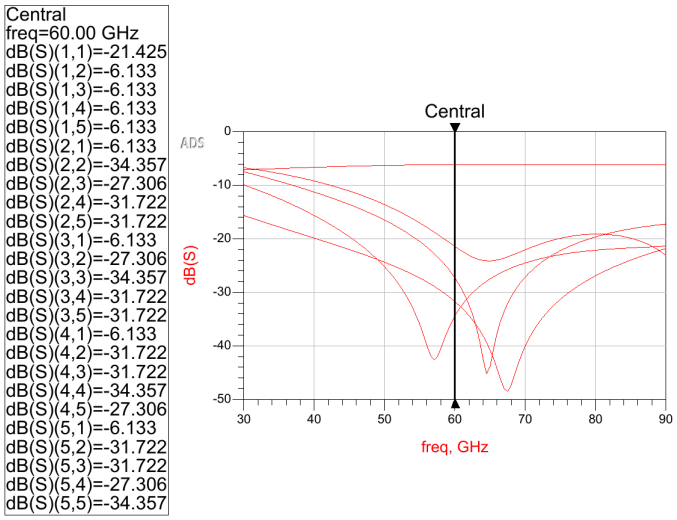

Fig. 3. S-parameter simulation for an "ideal layout" of 1:4 Webb Power Divider @ 60 GHz in the MnM substrate

III. LAYOUT AND SIMULATION

The layout of such a tiny circuit presented many challenges. The lines' width of each section were very different, and would not fit together as is. As a solution, another small section of line with a variable width was inserted in between the two other sections, as Figure 4 shows.

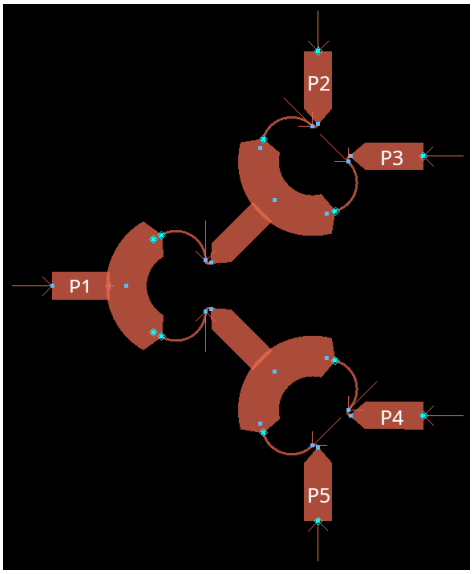

Fig. 4. Lines Layout for 1:4 Power Divider with 50Ω ports in the MnM substrate

Commercial alternatives for capacitors small enough to fit the gap between the lines could not be found. The adopted solution was to introduce a 3D interdigitated capacitor fabricated on the same substrate of the microstrip lines composing the circuit. Two dimensions were not enough to achieve the desired capacitance in the space given.

TABLE II
COMPARISON OF RECENTLY PUBLISHED POWER DIVIDERS WITH THIS WORK

Reference	This work	[2]	[3]	[10]
Technology	PCB (MnM Alumina)	PCB (Thin-Film Glass)	65nm CMOS	PCB (LTCC)
# of the N-way	4	2	4	2
Bandwidth [GHz]	$54 - 65(18\%)^*$	$26.5 - 29.5/37 - 40$	$20 - 44(75\%)$	$2 - 38(180\%)$
Project center frequency [GHz]	60	$28/39$	32	20
Insertion Loss [dB]	< 1	< 0.7	< 1.8	< 1.3
Isolation [dB]	> 11	> 12	> 14.5	> 17
Size $[mm^2]$	1.08	8.1	0.140	16

*Bandwidth was considered for frequencies in which Isolation[dB] > 11

This type of capacitor is widely used in mmWave applications [1], as they present adequate Q-factors and can be fabricated using conventional cheap technologies.

The constructed capacitor was based on a model that had already been realized by our laboratory using the MnM, which has been successfully used with high performance in mmWaves. A similar capacitance to the one needed had already been tested and a few adaptations were necessary to integrate the model to the rest of the layout.

The capacitor is made out of 4 fingers of $10\mu m$ x $75\mu m$ that span across the substrate's height ($50\mu m$), as shown in Figure 5. The capacitors should not be directly connected to ground, therefore, in the final layout, slots were introduced to the ground plane where the capacitors' walls would end.

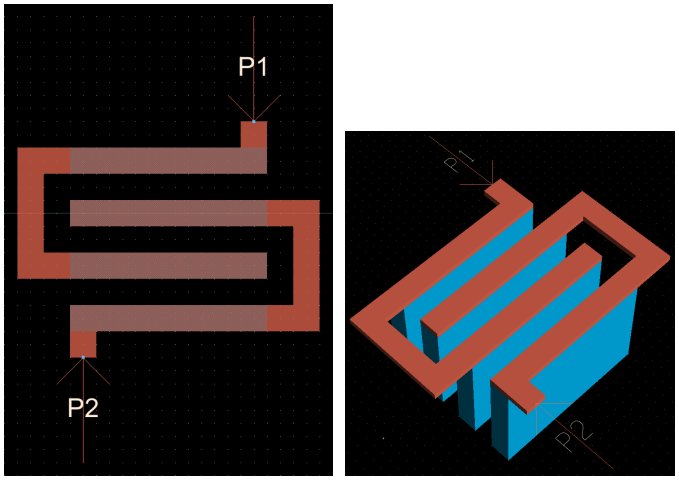

Fig. 5. 3D interdigitated capacitor layout for 60fF in the MnM substrate (Top-view and 3D-view)

As for the resistor, a rectangular-shaped line section of resistance $R_s = 100\Omega/sq$ properly sized was used to get 65Ω.

The final layout is shown in Figure 6, and its simulated S-parameters can be seen in Figure 7. The return loss in all ports (S(x,x)) is better than 14.5 dB db in all cases. The insertion loss between the input and each output (S(h,1) where h ranges from 2 to 5) is better than 0.877 dB. And the isolation between output ports (2 - 5) is better than 12.5 dB

The proposed Power Divider achieves a bandwidth of 11 GHz (18%) with good results for insertion loss ($< 0.9dB$) and acceptable port isolation ($> 11dB$) in compact-size

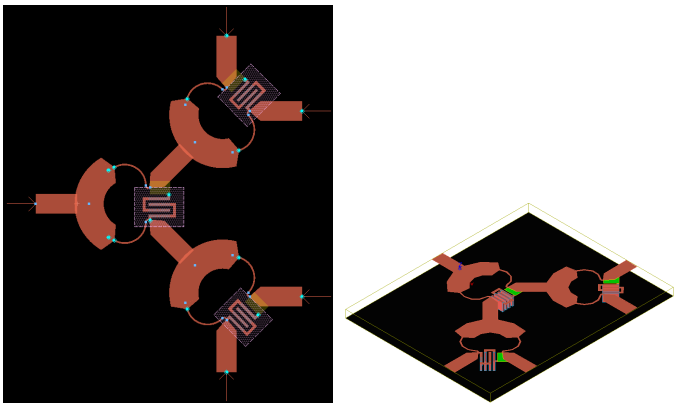

Fig. 6. Final Power Divider Layout (Top-view and 3D-view)

($1.08mm^2$) using cheap PCB technology.

IV. CONCLUSIONS

While CMOS alternatives might achieve a considerably smaller layout, it is also significantly more costly. Furthermore, in extremely high frequencies CMOS techonology, namely, transistors, do not work well, and other approaches have to be used instead, such as 3D integration using alternative substrates.

The proposed design may be a good option for a compact (considering PCB technology) and cheap (in comparison to CMOS) power divider in mmWave application using cheap techonology.

Manufacturing and tests are necessary to gather real-life parameters and prove the usability of the layout, but simulation results seem promising.

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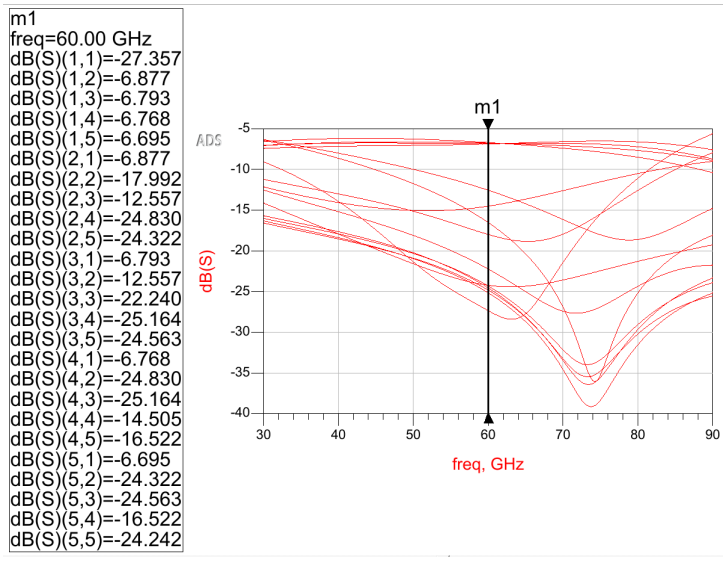

Fig. 7. Simulated S-parameters for the final layout

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