A Static 4:1 Frequency Divider up to 16 GHz in 120 nm CMOS

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Abstract— A completely integrated 16 GHz static 4:1 frequency divider in 120 nm CMOS is presented. The divider operates up to 16 GHz and features an enhanced input sensitivity of 0 dBm over a broad input band of 14 GHz. The circuit draws 60 mA from a single 1.5 V supply. To drive 50 Ω loads up to 4 GHz, an output buffer is also included in the divider circuit.

I. Introduction

HIGH speed static frequency divider ICs are critical functional blocks in a variety of applications, ranging from RF instrumentation to broadband optical fiber communication systems. For these systems maximum speed and high level of integration is mandatory, while power consumption is not a limiting factor. To date, impressive results have been achieved only with realizations in InAlAs/InGaAs and SiGe bipolar with frequencies up to 100 GHz. In contradiction CMOS frequency dividers have achieved only maximum operation frequencies in the range of 10 GHz [1-5]. However, the fastest of these dividers use dynamic circuits [1], [2], injection-locked oscillators [3] or impractical modified logic [4], [5] which requires external biasing at the clock inputs for various signal levels.

We developed a stand alone frequency divider, required for high speed data communication systems. This circuit is optimized for high speed and high sensitivity operation, while still using static CML logic for maximum bandwidth. Inputs and outputs are designed for differential operation in a 50 Ω measurement system.

II. Circuit Design

Figure 1 shows the block diagram of the 4:1 static frequency divider. The internal dividing function is based on master-slave D-type flip-flops by connecting the inverted slave outputs to the master inputs. A separate buffer decouples the divider core from the 50 Ω surrounding. Differential signals provide sufficient noise margin even with reduced voltage swings. For high speed operation, the well-proven CML principle is used, which decreases the internal voltage swing and therefore guarantees high operation frequencies.

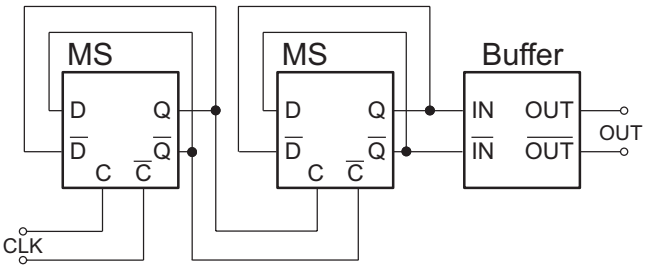

Fig. 1. Block-diagram of a 4:1 static frequency divider

In figure 2 the divider core, containing the master-slave flip-flop is shown. The clock input stage matching is realized with 100 Ω on-chip resistors, connected to a DC level shifter. A DC level of about VDD/2 is best for fast switching and is used in the first master-slave flip-flop. Between the first and the second master-slave flip-flop, source follower are used for decoupling and for level shifting. All

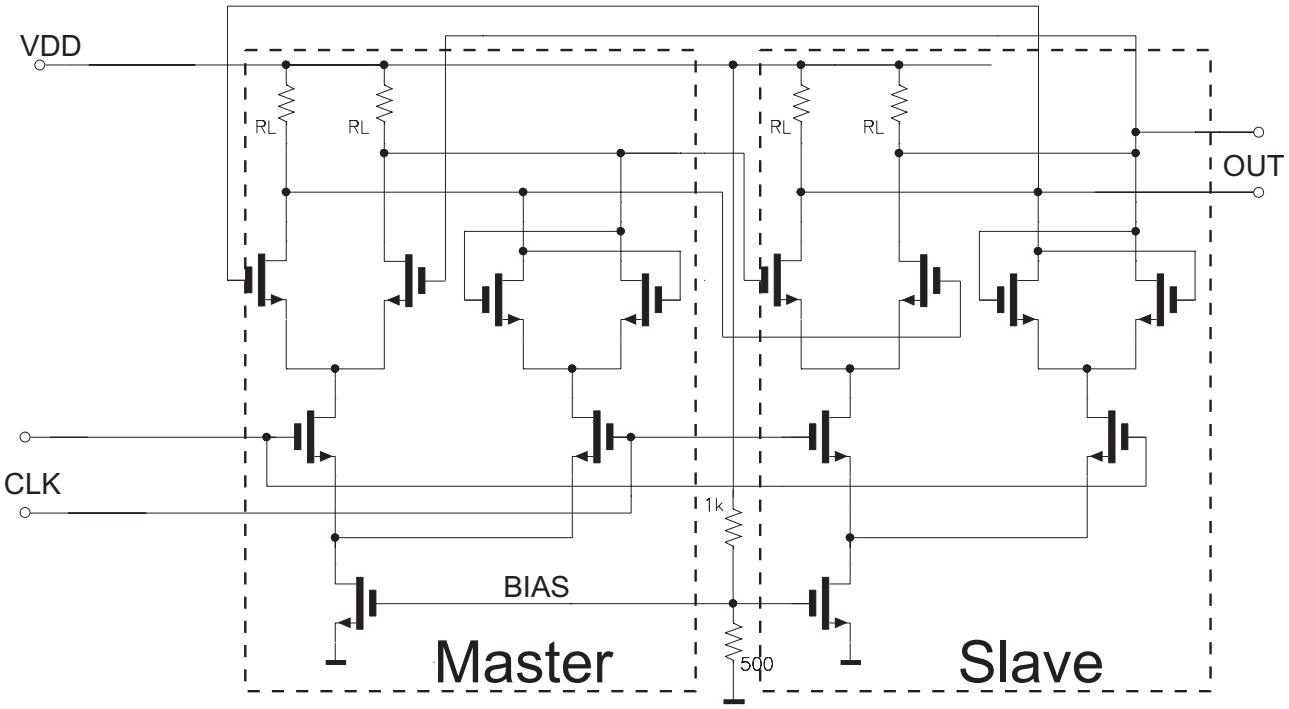

Fig. 2. Divider core circuit diagram

transistors in the latches are of the same size and are low V_T NMOS devices, because of their higher speed compared to PMOS transistors. Relatively large devices are used to increase input sensitivity. 100 Ω Poly-silicon resistors (RL) are used as low capacitive loads for the latches. The simulated internal voltage swing is typical two times 650 mV_{pp}.

Since a differential design is applied, the layout is kept as symmetrical as possible. Furthermore all interconnects are kept as short as possible. Especially the lines between slave outputs and master inputs are affecting the maximum operation frequency, because of their propagation delay and capacitive load.

The multiple stage output buffer in figure 3 is used to create sufficient output voltage swing. It consists of a pair of source followers and two amplifier stages. In each stage the tail current is twice the current of the previous stage. The last differential amplifiers are designed to provide enough voltage swing over the 25 Ω total load. The differential outputs are terminated with on-chip 50 Ω resistors. This on-chip matching resistors reduces output reflections and therefore allow broadband operation up to very high frequencies.

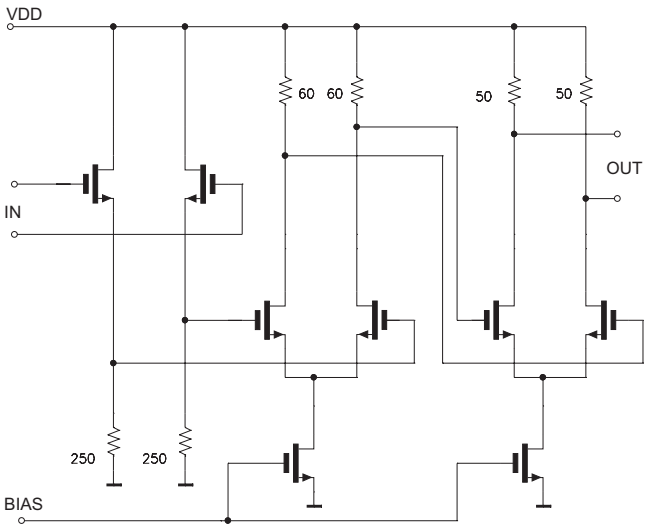

Fig. 3. Output buffer circuit diagram

III. Technology

The circuits is fabricated in a 120 nm CMOS technology with six-layer copper metallization and normal silicon-oxide dielectric ($\varepsilon_r = 3.9$). The chip size is mainly 0.47 x 0.49 mm^2. The chip size is determined by the pad frame and not by the active area, which is only a fraction of the total chip area. Figure 4 shows the layout of the static frequency divider. During fill structures in all

metal layers, a chip-photo could not be displayed. The manufactured NMOS transistors have a cut of frequency f_T of 100 GHz and a maximum oscillation frequency f_{max} of 50 GHz respectively [6].

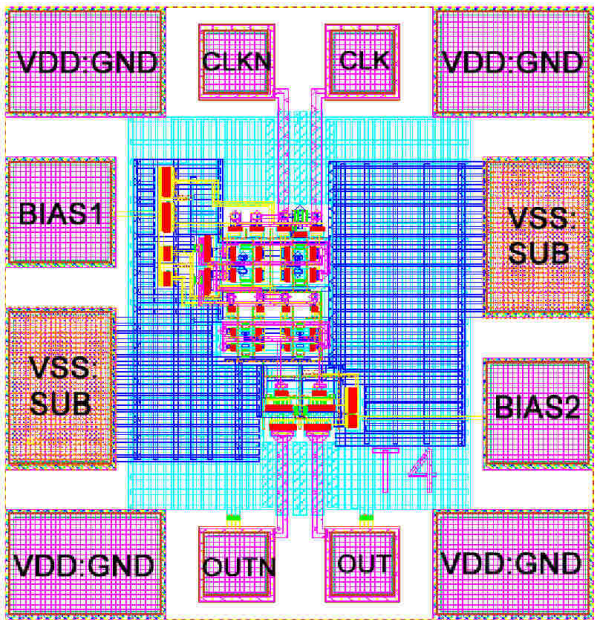

Fig. 4. Chip layout ($0.47 \times 0.49\,\mathrm{mm}^2$)

IV. Experimental Results

To evaluate the circuit performance the chip was mounted on a 30x30mm^2 0.51mm RO4003 microwave substrate ($\varepsilon_r = 3.38$) with SMA connectors for input and output signals. Figure 5 shows this evaluation board mounted on a special high frequency test fixture. The measured data represents the performance of the divider and includes the loss caused by the bond wires, microstrip lines on the test board, RF connectors and the 180^o hybrid coupler. The differential input signal was generated by a 180^o hybrid coupler.

Figure 6 gives the input sensitivity versus input frequency. The circuit shows broadband performance up to operation frequencies of nearly 14 GHz with input levels of 0 dBm. At 1.5 V power supply a maximum operation frequency of 16 GHz is achieved. The slightly higher operating frequency could be achieved at an increased power supply of 1.8 V. The highest input sensitivity is measured at 10 GHz. The loss of sensitivity below 1 GHz is caused by the lower cut off frequency of the hybrid coupler and the limited slew rate of the sinussoidal input signal. At low frequencies a square wave signal should be applied, to reach the maximum bandwidth.

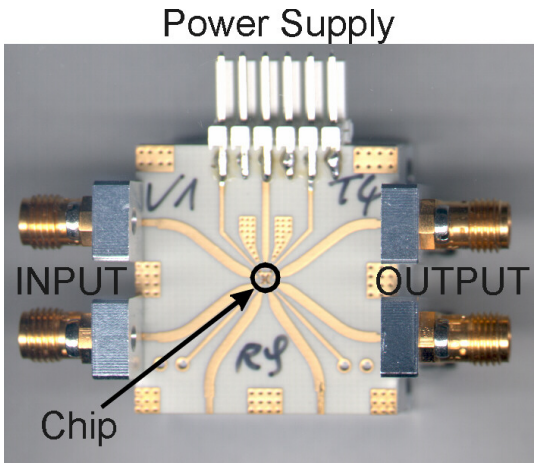

Fig. 5. Divider 30x30mm^2 high frequency test fixture

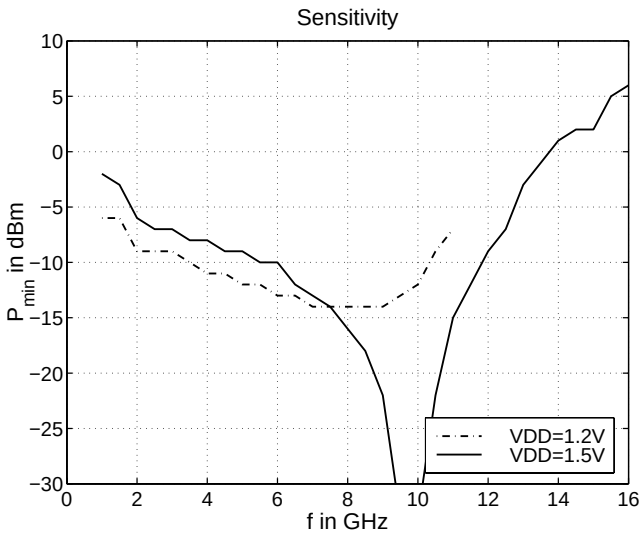

Fig. 6. Measured divider sensitivity versus input power

Figure 7 shows the input (top) and output (bottom) transient signals at 15 GHz input frequency. The measured single-ended output voltage swing on an external 50 Ω load is typical two times 220 mV$_{pp}$.

The divider supply current is 27 mA at 1.2 V and 60 mA at 1.5 V. Because the flip-flop and the output buffer share the VSS and VDD pads, the individual currents could not be measured. According to simulation results, the divider core draws 34 mA and the output buffer 26 mA from a single 1.5 V supply. At this supply voltage, the divider consumes 90 mW.

V. Conclusions

We have presented a fully integrated high speed 4:1 frequency divider in 120 nm standard CMOS, which operates up to 16 GHz. The divider features high input sensitivity,

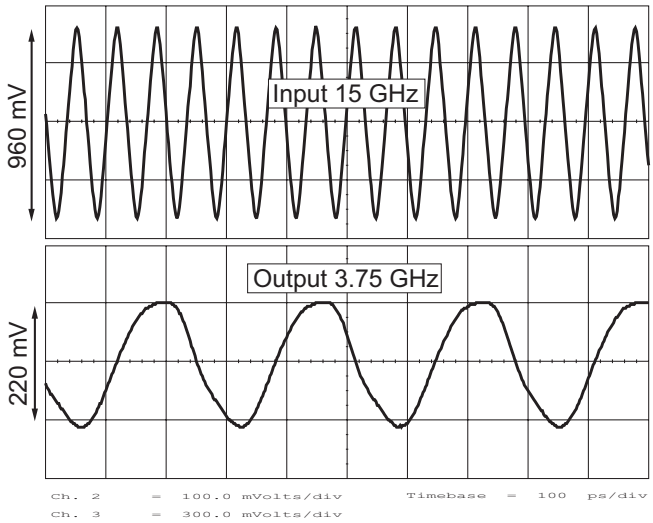

Fig. 7. Measured single ended input and output waveforms at 15 GHz

50 Ω output buffer and does not require any external adjustments. This is the highest reported value to date for a CML full static 4:1 frequency divider realized in a CMOS technology. For comparison, one of the best published value for a standard CML logic (more the 2:1) frequency divider in CMOS technology is 12 GHz [5].

Acknowledgments

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