25 GHz Monolithic Oscillator with Frequency Divider in SiGe Bipolar Technology

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Abstract ***This paper presents a monolithic voltage-controlled oscillator with static frequency divider in a pre-production 0.4 μm SiGe bipolar technology for broadband communication applications. The voltage-controlled oscillator operates from 17.8 GHz to 25 GHz. The division ratio of the static frequency divider is 16. The circuit consumes 500 mW from the 5 V supply including the two output buffers.***

I. Introduction

The demand for wireless services will increase rapidly within the next few years. Wireless local area networks (WLANs) at 2.4 GHz, 5.2 GHz, and 17.2 GHz, satellite communications systems at 8 GHz and 10 GHz, and radio links at 13, 15, and 18 GHz are examples for wireless systems up to 20 GHz. Above 20 GHz, point-to-multipoint systems between 24.5 and 29.5 GHz, local multipoint distribution systems (LMDS) at 28 and 38 GHz, and European microwave video distribution systems (MVDS) at 42 GHz are emerging. In all these wireless systems frequency synthesizers are needed.

For the mobile communications market with operating frequencies up to 2.5 GHz highly integrated circuits are available from many manufacturers. These dividers, dual-modulus prescalers, and PLL-ICs (consisting of programmable dividers and phase detectors) for frequency synthesis are mostly fabricated in low-cost technologies like silicon bipolar, CMOS or BiCMOS.

Key building blocks to achieve carrier frequencies beyond 20 GHz are the voltage-controlled oscillator and the frequency divider. In this paper we demonstrate the monolithic integration of these two RF key building blocks for operating frequencies beyond 20 GHz. Combining these two blocks with already existing designs of PLL-ICs (e.g. [1], etc.) completely integrated frequency synthesizers for frequencies beyond 20 GHz would be feasible. Up to now commercially available ICs with integrated VCOs with frequency dividers achieve 15 GHz in GaAs Technology [2].

Fig. 1 shows a typical frequency synthesizer solution in phase-locked loop (PLL) architecture. The voltage-controlled oscillator (VCO) operates at the desired output frequency. The prescaler divides the VCO frequency into the much lower frequency range which can easily be handled by commercially available PLL-ICs mentioned above.

Highly integrated Si-based synthesizers with VCO, frequency divider and phase detector on chip achieve operating frequencies around 7 GHz [3]. The highest operating frequency for completely integrated synthesizers reported is 34 GHz [4] realized in III-V semiconductor technology.

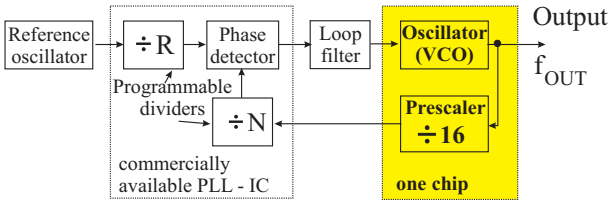

Fig. 1. Block diagram of frequency synthesizer in phase-locked-loop architecture

This work presents a monolithic IC suitable for frequency synthesis consisting of a voltage-controlled oscillator with divide-by-16 static frequency divider for broadband wireless applications between 18 GHz and 25 GHz. The circuit is fabricated in a low-cost 0.4 μm/85 GHz SiGe bipolar technology. By combining the integrated circuit with a frequency doubler, LMDS applications at 38 GHz and MVDS applications at 41 GHz can be handled.

II. Circuit Design

Fig. 2 shows the block diagram of the monolithic VCO with static frequency divider. All blocks are designed in fully differential logic. The two output buffers have

balanced outputs, each of the buffers can drive a 50 Ω load.

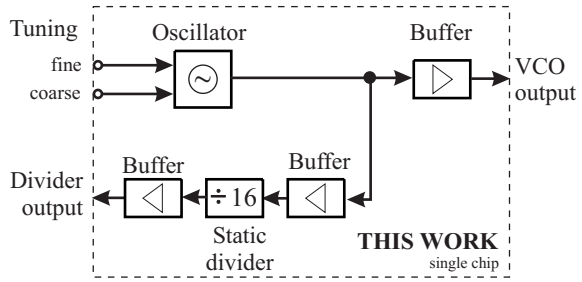

Fig. 2. Block diagram of the monolithic VCO with static frequency divider

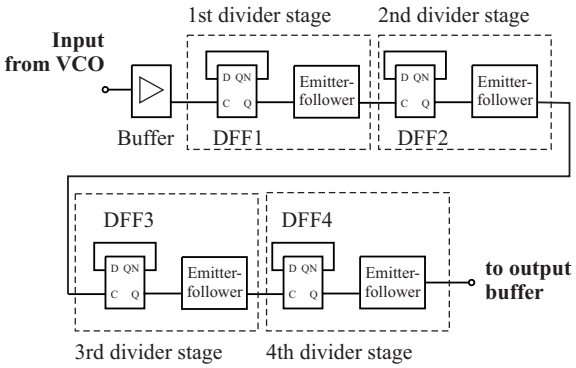

Fig. 4. Block diagram of the static divide-by-16 frequency divider

A. Voltage-Controlled Oscillator

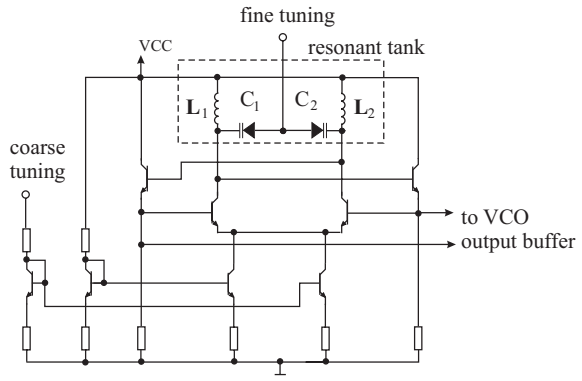

Fig. 3. Schematic of the voltage-controlled oscillator

Fig. 3 shows the VCO topology. The oscillator consists of a cross-coupled differential amplifier loaded with a resonant LC circuit. Emitter followers in the feedback path help to reduce the loading of the resonant circuits by the input of the differential amplifier and achieve a high loaded Q of the resonator. On-chip spiral inductors and transistors used as varactors build the resonant circuits. A coarse tuning of the output frequency of the oscillator can be performed by varying the operating current of the oscillator [3].

B. Static Frequency Divider

The block diagram of the divide-by-16 static frequency divider is shown in fig. 4. The divider input buffer is realized with a differential amplifier and emitter followers for level shifting.

The static frequency divider consists of 4 D-type master-slave flip-flops (DFFs) and emitter followers for level shifting. The transistors of the first flip-flop operate at the optimum current density for peak transit frequency. As the operating frequencies of the following flip-flops always decrease by the factor of two, their operating currents are reduced stage by stage to save power. The divider output buffer is implemented as differential amplifier.

C. Simulated Current Consumption

The simulated total current consumption of the circuit was 96 mA at the 5 V supply. Fig. 5 shows the simulated current distribution of the building blocks at the supply voltage of 5 V.

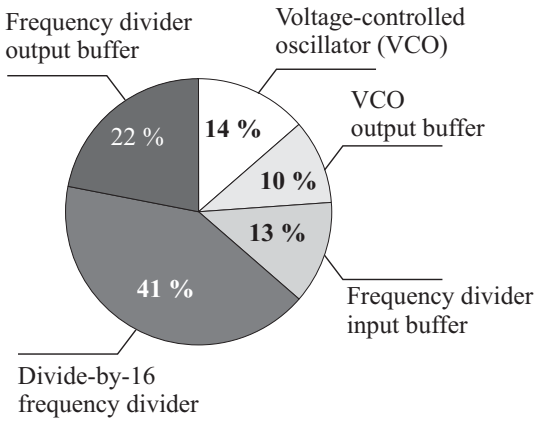

Fig. 5. Current distribution of the circuit at 5 V supply voltage simulated. Total current: 96 mA.

III. Semiconductor Technology

The circuit was fabricated in a pre-production 0.4 μm-SiGe bipolar technology [5] using a double-polysilicon self-aligned emitter-base configuration with effective emitter width of 0.2 μm. Fig. 6 shows a schematic cross section of a npn-transistor. The transis-

tors manufactured in this technology offer a maximum transit frequency of 85 GHz, maximum oscillation frequency of 128 GHz, and CML gate delay time of 6.8 ps. The four available metallization layers enable low parasitic wiring capacitances. Fig. 7 shows the chip photograph of the monolithic VCO with static divide-by-16 frequency divider.

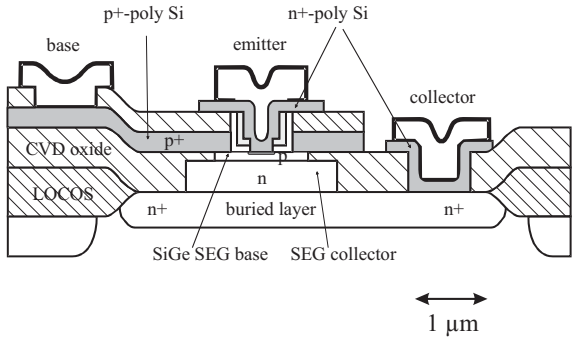

Fig. 6. Schematic cross section of a npn-transistor

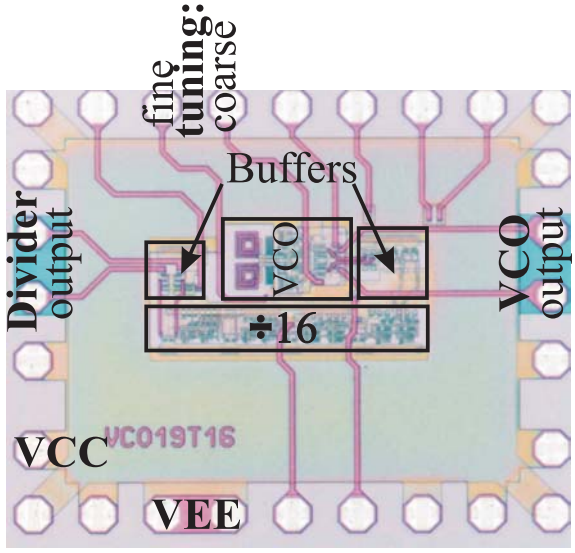

Fig. 7. Chip photograph (size: 860 μm x 700 μm)

IV. Experimental Results

All measurements were performed with wirebonded chips mounted on high-frequency ceramic substrates with $\epsilon_r = 9.9$ and thickness of 0.31 mm. Fig. 8 shows the photograph of the test fixture.

The total power consumption of the circuit is 500 mW at the supply voltage of 5 V and includes the power consumption of the VCO, the static divide-by-16 frequency divider, the buffer between the VCO and the divider, and the two output buffers driving 50 Ω loads.

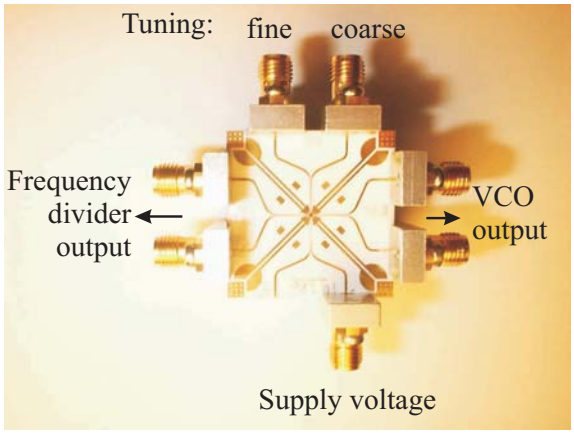

Fig. 8. Test fixture (size: 3 cm x 3 cm)

Fig. 9 shows the coarse tuning characteristic of the VCO . The VCO operates in the output frequency range between 17.8 GHz and 25 GHz. The fine tuning range is at least 2 GHz.

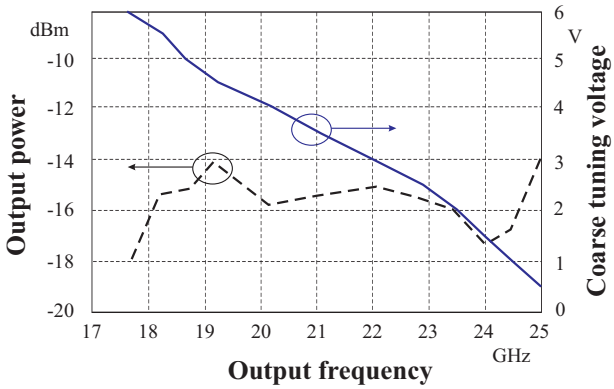

Fig. 9. VCO tuning characteristic

The spectrum of the output signal at 21 GHz is presented in fig. 10. Without de-embedding of the losses of the cable and the hybrid coupler, the output power of the circuit is -14 dBm at 19 GHz, and -15.8 dBm at 21 GHz. The VCO has a phase noise of -86 dBc/Hz at 1 MHz offset from 21 GHz output frequency .

Fig. 11 shows the output waveforms of the circuit for the VCO output frequency of 21 GHz and the division ratio of 16. The amplitude of the divide-by-16 single-ended output signal is > 400 mV$_{PP}$, sufficient to drive PLL-circuits. Table I summarizes the technical data of the circuit.

Level of monolithic integration	VCO with static frequency divider
Semiconductor Technology	0.4 μm/85 GHz-f_T SiGe bipolar
Power consumption	500 mW @ 5 V
Output frequency range	17.76 GHz - 25 GHz
VCO output power	-14 dBm ... -18 dBm
Divider output voltage swing	> 400 mV$_{PP}$
Phase noise @ 21 GHz	-86 dBc/Hz @ 1 MHz offset
Chip size	0.86 $\times$ 0.7 mm^2

TABLE I. Technical data

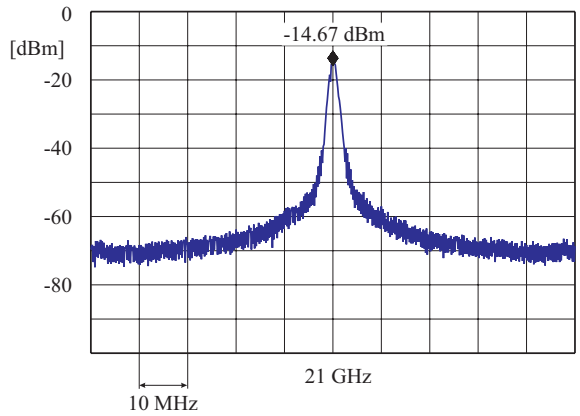

Fig. 10. Spectrum of the VCO output signal at 21 GHz without de-embedding of the measurement equipment losses

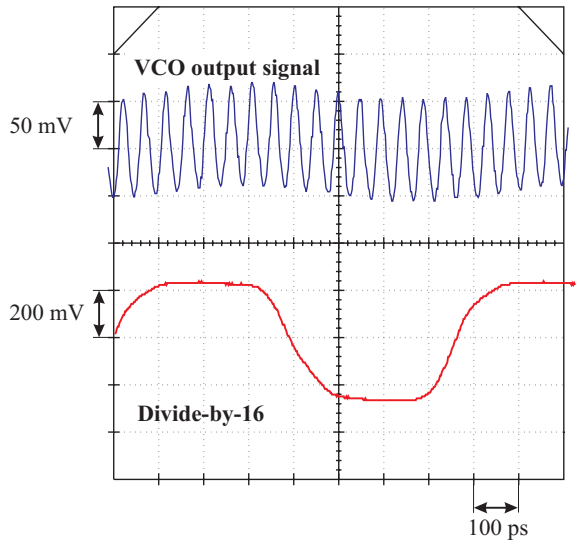

Fig. 11. Output waveforms
Upper curve: VCO waveform f_{VCO}= 21 GHz ,
Lower curve: Divider waveform: f_{VCO} / 16
(single-ended)

V. Conclusions

A monolithic voltage-controlled oscillator (VCO) with static frequency divider in a pre-production 0.4 μm SiGe bipolar technology for broadband applications between 18 GHz and 25 GHz is presented. The division ratio of the static frequency divider is 16. The power consumption of 500 mW @ 5 V supply includes the consumption of the VCO, of the frequency divider with input buffer, and of the two output buffers. To our knowledge the operating frequency of 25 GHz is state of the art for silicon-based monolithically integrated VCOs with frequency dividers.

References

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