An Initial Discussion of an Adaptive Impedance Matching Circuit for PLC Systems

Luis Guilherme da S. Costa, Vinícius L. R. da Costa, Ândrei Camponogara, and Moisés Vidal Ribeiro

***Abstract*— This paper proposes an adaptive impedance matching coupling circuit for power line communication (PLC) systems operating in the frequency band of 1.7 up to 50 MHz. The proposed PLC coupling circuit is designed based on an analog filter bank approach. The simulation results show that the proposed analog filter bank approach can provide low return loss and high insertion gain in the band-pass. In general, the attained results point out that the proposed circuit constitutes an interesting research direction to improve the impedance matching between PLC transceivers and electric power grids.**

***Keywords*— Power line communication, coupling, impedance matching, analog filter, electric power grids.**

I. Introduction

Power line communication (PLC) is an attractive data communication technology since it allows the use of the existent electric power infrastructure as data communication medium. However, electric power grids are a harsh medium for transmitting data-carrying signals due to the interference related to the use of electromagnetically unshielded power cables, signal attenuation caused by distance and frequency increase, multipath effect, and high power impulsive noise generated by switching devices [1]. Furthermore, the dynamic switching behavior of loads degrades the maximum power transfer between PLC transceivers and electric power grids [2].

In the literature, few contributions address the impedance mismatching between PLC transceivers and electrical power grids [3], [4] since it is arduous to control the dynamic switching of loads in electric power grids. Note that due to this loads dynamic, the input impedance of the electric power circuit varies in time and frequency domains. Beyond of that, PLC coupling circuits are subject to the fluctuations of the electric power grid topology combined with unknown cable characteristics and changes in the loads connected to the electric power grid. Such a scenario makes difficult to match the impedance between PLC coupling circuits and electric power grids.

Recent results recommend adaptation of the input impedance of the PLC coupling circuit to ensure that it is approximately equal, on average, to the input impedance of the electric power grid. Note that the input impedance of the PLC coupling circuit is selected by the winding ratio $1:N$ through an broadband radio frequency (RF) transformer [5]. In [6], the authors designed two PLC coupling circuits incorporating $4:1$ and $2:1$ winding ratios for the permanent connection between PLC coupling circuits in the electric power grids for maximum power transfer.

In order to improve the impedance matching between PLC transceivers and electric power grids, this paper proposes a capacitive, single-input single-output (SISO), and low-voltage (LV) PLC coupling circuit with an adaptive impedance matching in the frequency range $2-50$ MHz based on the use of an analog filter bank approach. Observe that our proposed PLC coupling circuit measures the received signal strength and compares it with a typical value stored in a microcontroller unit. The microcontroller analyzes which analog filter offers the maximum voltage signal strength at the input of its analog-digital converter (ADC) and then switches the radio frequency micro-electro-mechanical switches (RF MEMS) guaranteeing maximum power transfer at the ADC. Afterwards, the microcontroller starts a process of monitoring the signal strength by the ADC. If the strength of this signal decreases, a new analysis process is started by the microcontroller to check which analog filter provides the best signal strength.

II. Problem Formulation

Considering electric power grids as time-varying systems, we can use the two-wire transmission line theory to adapt two-port $ABCD$ matrices for modelling the signal propagation and analyzing impedance mismatching [7] in a time-varying scenario. In this regard, the model based on the $ABCD$ matrix shown in Fig. 1 can be used to analyze the impedance mismatching problem related to PLC systems. This model emphasizes that electric power grids and PLC coupling circuits are time-varying systems. Note that the time-varying behavior related to electric power grids is mainly associated with dynamics of loads owned by electric utilities and consumers.

According to Fig. 1, we have

$$\begin{bmatrix} V_1(f,t) \\ I_1(f,t) \end{bmatrix} = \begin{bmatrix} A(f,t) & B(f,t) \\ C(f,t) & D(f,t) \end{bmatrix} \begin{bmatrix} V_2(f,t) \\ I_2(f,t) \end{bmatrix}, \quad (1)$$

in which $V_{TX}(f,t)$ is the voltage source with internal impedance $Z_{TX}(f,t)$; $V_1(f,t)$ and $I_1(f,t)$ are respectively the voltage and current at the input port of the electric power circuit; $V_2(f,t)$ and $I_2(f,t)$ are respectively the voltage and current at the output port of the electric power circuit; $V_{RX}(f,t) = V_2(f,t)$ is the voltage at the input port of the transceiver; $Z_{RX}(f,t)$ is the impedance at the input port of the PLC

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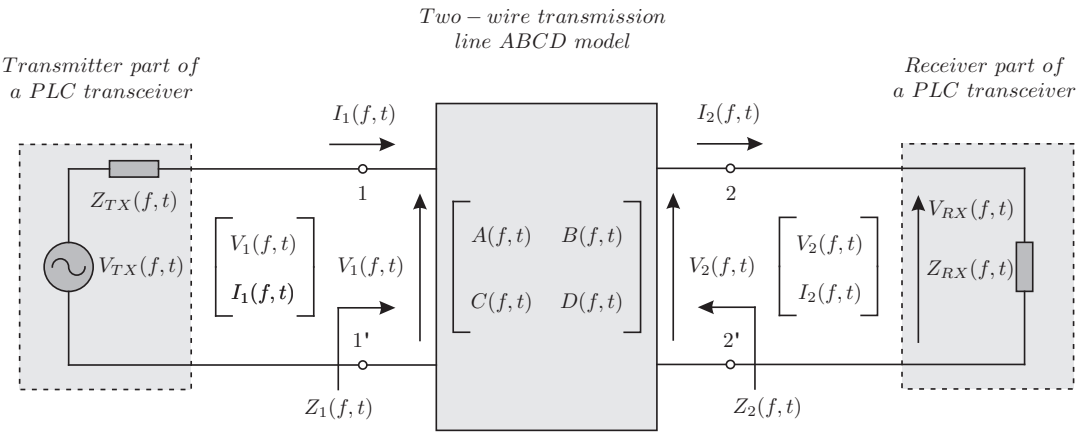

Fig. 1: Two-port $ABCD$ time varying matrix model for dealing with the dynamic of electric power grids.

transceiver; and $Z_1(f,t)$ and $Z_2(f,t)$ are the input impedance at the input and output port of the electric power circuit, respectively. Note that $V_1(f,t) = V_{TX}(f,t) - Z_{TX}(f,t)I_1(f,t)$ is the voltage at the input port of the two-port $ABCD$ of the electric power circuit. The voltage $V_{RX}(f,t)$ at the receiver of the PLC transceiver, which has an impedance $Z_{RX}(f,t)$, is given by

$$V_{RX}(f,t) = V_2(f,t) = Z_{RX}(f,t)I_2(f,t). \tag{2}$$

The relations between the input and output ports of the two-wire transmission line shown in Fig. 1 can be obtained using

$$\begin{aligned} V_1(f,t) &= A(f,t)\,V_2(f,t) + B(f,t)\,I_2(f,t) \\ I_1(f,t) &= C(f,t)\,V_2(f,t) + D(f,t)\,I_2(f,t). \end{aligned} \tag{3}$$

Observe that the two-port network can be written as a function of the input impedance parameter, $Z_1(f,t)$, related to the electric power circuit. It can be obtained with the time-varying $ABCD$ matrix, see (1). As a result,

$$Z_1(f,t) = \frac{V_1(f,t)}{I_1(f,t)} = \frac{A(f,t)\,Z_{RX}(f,t) + B(f,t)}{C(f,t)\,Z_{RX}(f,t) + D(f,t)}. \tag{4}$$

It means that the input impedance parameter of the electric power circuit depends on the time-varying behavior of input impedance $Z_{RX}(f,t)$ of the PLC transceiver and the $ABCD$ matrix of the electric power circuit [8]. Thus, we can conclude that to maximize the power transfer from the transmitter to the receiver, the PLC coupling circuit must be designed to precisely match the time-varying behavior of the impedance of input and output ports of an electric power circuit. Also, such circuit is modeled as a time-varying $ABCD$ matrix, with the $Z_{TX}(f,t)$ and $Z_{RX}(f,t)$ impedances of the PLC transmitter and receiver, respectively.

At this moment, it is important to emphasize that the impedance of electric power grids is continuously changing as time evolves. Consequently, it is challenging to achieve perfect impedance matching if $Z_{RX}(f,t)$ and $Z_{TX}(f,t)$ are not designed by taking into account the time variable, t, (i.e., the time-varying behavior of electric power grids). Based on this scenario, it is clear that the impedance matching between PLC transceivers and electric power grids demands the design of adaptive PLC coupling circuits that are capable of detecting variations of the impedance of electric power grids and dynamically adjust the impedance of the coupling circuit.

III. Analog Filter Bank Approach for Impedance Matching

The impedance matching between PLC transceivers and electric power grids can be implemented by using a bank of J impedance matching circuits. To illustrate it, the block diagram of the so-called impedance matching circuit bank for PLC transceivers is shown in Fig. 2.

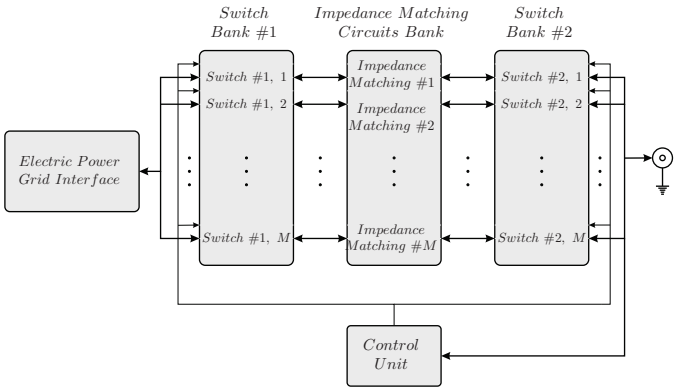

Fig. 2: Block diagram of the impedance matching circuits bank for a PLC transceiver.

The impedance matching circuit bank can be divided into four main parts: electric power grid interface, switch banks, impedance matching circuit bank, and control unit. Based on the summation of the signal available at the output load of the Switch Bank #2, the Control Unit applies a control strategy to simultaneously control the Switch Banks #1 and #2 in order to ensure that the matching impedance is accomplished in a time interval. Using the Control Unit and the Switch Banks #1 and #2, the impedance matching can be accomplished by using the following strategy: all impedance matching circuits are designed to match the input impedance associated with the band of 2 - 50 MHz and then the impedance matching can be easily carried out with well-known techniques. This strategy will offer an impedance matching performance that depends on the frequency selectivity of the input impedance of the electric power grid in the whole frequency band. On the other hand, it can remarkably demand less hardware complexity.

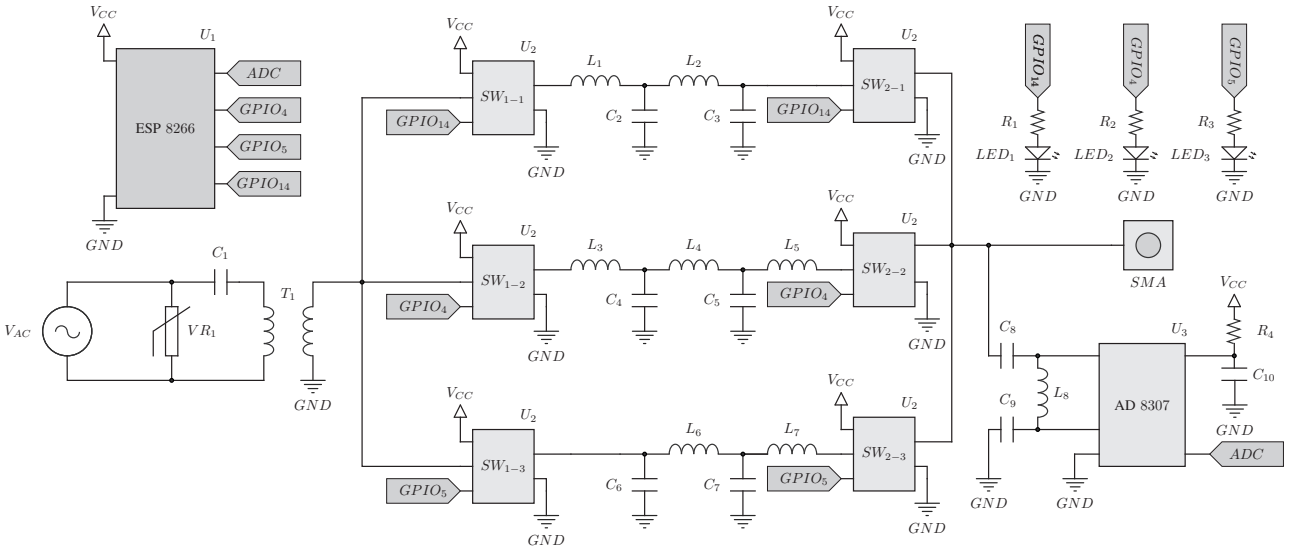

Fig. 3: Schematic of the adaptive, broadband, capacitive, SISO, and LV PLC coupling circuit with $J = 1$ and $M = 3$.

IV. Validation through a Prototype

Fig. 3 shows the schematic of an adaptive, broadband, capacitive, and SISO PLC coupling circuit for LV electric power grids operating in the frequency band of $2 - 50$ MHz. Following the schematic of the adaptive impedance matching coupling circuit proposed in Fig. 3, one can see that the component V_{R1}, is the gas discharge tube (GDT) protector, which aims to protect the adaptive impedance matching coupling circuit against over-voltage and over-current transients from the electric power grid. The C_1 capacitor performs a high-pass filtering so that the 3 dB cut-off frequency is designed for 1.7 MHz and then blocks the fundamental frequency of 60 Hz of the electric power grid. Moreover, the RF transformer T_1, with ratio of $1 : 1$, is responsible for galvanic isolation. It is usually necessary when two or more electric power circuits are connected and their grounds may be at different potentials. Notice that T_1 is an effective approach for breaking ground loops by preventing undesirable current flowing between two distinct circuits sharing a ground conductor. Moreover, when an over-voltage transient occurs in the electric power grid, the RF transformer core may saturate resulting in a reduced voltage transfer from the electric power grid to the front-end circuit of the PLC transceiver. In this case the RF transformer provides electric protection.

Furthermore, regarding the RF MEMS switch banks (SW_{1-1}, SW_{2-1}, SW_{1-2}, SW_{2-2}, SW_{1-3}, and SW_{2-3}), note that their primary purpose is to route signals through the analog filters with the lowest insertion loss, the highest return loss, and the highest isolation between the interface with the electric power grid and the output load of the adaptive impedance matching coupling circuit (i.e., the analog filter bank). Only two switches are selected in an operational state, and only one analog filter of the adaptive impedance matching coupling circuit bank is used, while the other $M - 1$ switches present a high impedance in their ports. It is important to observe that the RF MEMS switch banks always work together by selecting one of the analog filter bank in the following sequence SW_{1-1} with SW_{2-1}, or SW_{1-2} with SW_{2-2}, or SW_{1-3} with SW_{2-3}. The analog low-pass filter banks designed with impedance relation $1 : 2$ (L_1, L_2, C_2, and C_3), $1 : 1$ (L_3, L_4, L_5, C_4, and C_5), and $2 : 1$ (L_6, L_7, C_6, and C_7) connected between the RF MEMS switches are used to match the impedance between the output load and the electric power grid.

Moreover, according to Fig. 3, the component U_3 is the logarithmic amplifier (AD8307) used for sensing the strength of the voltage signal at the output load of the switch banks. The components C_8, C_9, and L_8, which are connected in the input of the logarithmic amplifier U_3, are a narrowband filter designed to detect the frequency of the maximum gain of the analog filter. The microcontroller U_1 ESP-8266 controls all the RF MEMS switches, through the general purpose input/output (GPIO) pins ($GPIO_4$, $GPIO_5$ and $GPIO_{14}$). These pins are responsible for selecting the filter in which the best impedance matching is achieved after the analysis processed by the microcontroller. The LEDs, LED_1, LED_2, and LED_3 indicate which filter is selected between the electric power grid and the output load.

For an appropriate design of the impedance matching circuits bank (i.e., analog filter bank), it is necessary to know the input impedance values of electric power grids. According to [9], 90% of the input impedance values measured are between 25 Ω and 100 Ω with mean value equal to 50 Ω. Therefore, three analog filters ($M = 3$) are designed with the input impedance equal to 25 Ω, 50 Ω, and 100 Ω. These three analog filters are designed considering input and output impedance ratios of $1 : 2$ (25 Ω to 50 Ω), $1 : 1$ (50 Ω to 50 Ω), and $2 : 1$ (100 Ω to 50 Ω), where 50 Ω is the output load impedance of the PLC transceiver, according to Fig. 3. Also, first (25 Ω to 50 Ω) and third (100 Ω to 50 Ω) analog filters are low-pass irregular ones, while the second analog filter (50 Ω to 50 Ω) is a low-pass Chebyshev one. Note that the output load impedance of the analog filter must be matched to 50 Ω for ensuring $1 : 2$, $1 : 1$, and $2 : 1$ ratios.

The propose is to design a low-pass filter with approximation function for broadband impedance matching, which results in low-pass irregular analog filters of even order. These types of analog filters are useful to perform impedance matching when the frequency band is broad.

V. Simulation and Analysis

This section presents simulation results regarding the scattering parameters (i.e., reflection parameters, $S_{11}(f)$ and $S_{22}(f)$, and transmission parameters, $S_{12}(f)$ and $S_{21}(f)$) obtained for the analog filters, which were designed to constitute the prototype of the adaptive PLC coupling circuit. Such results are computed by using the software Advanced Design System (ADS) considering the frequency band $0-100$ MHz. Observe that the knowledge of this parameters are at most importance to understand the behavior of the PLC coupling circuit.

Fig. 4 shows the magnitudes of the scattering parameters computed for the analog filters. Also, Figs. 4a and 4c refer to the low-pass irregular analog filters with an input impedance of 25 Ω and 100 Ω, respectively, while Fig. 4b refers to the low-pass Chebyshev analog filter. Note that the magnitudes of $S_{12}(f)$ and $S_{21}(f)$ are around 0 dB. Also, the low-pass Chebyshev analog filter offers a better roll-off factor and a stop-band attenuation 11 dB higher than the low-pass irregular analog filters in 100 MHz. Concerning the magnitude of $S_{11}(f)$ and $S_{22}(f)$, we see that the low-pass irregular analog filters achieve a better impedance matching in the middle of the frequency band, see Figs. 4a and 4c. Also, the low-pass irregular analog filter with input impedance of 100 Ω, see Fig. 4c, shows the lowest magnitudes of $S_{11}(f)$ and $S_{22}(f)$ (e.g., -22 dB in 25 MHz and 36 MHz) while the low-pass Chebyshev analog filter achieves magnitude of $S_{11}(f)$ and $S_{22}(f)$ equal to -10 dB in 40 MHz. Magnitudes of $S_{11}(f)$ and $S_{22}(f)$ equal to -31 dB and -33 dB are observed in 29 MHz and 48 MHz, respectively, when the low-pass Chebyshev analog filter is applied. Overall, the best impedance matching is obtained for $100-50$ Ω while the worst is found for $25-50$ Ω.

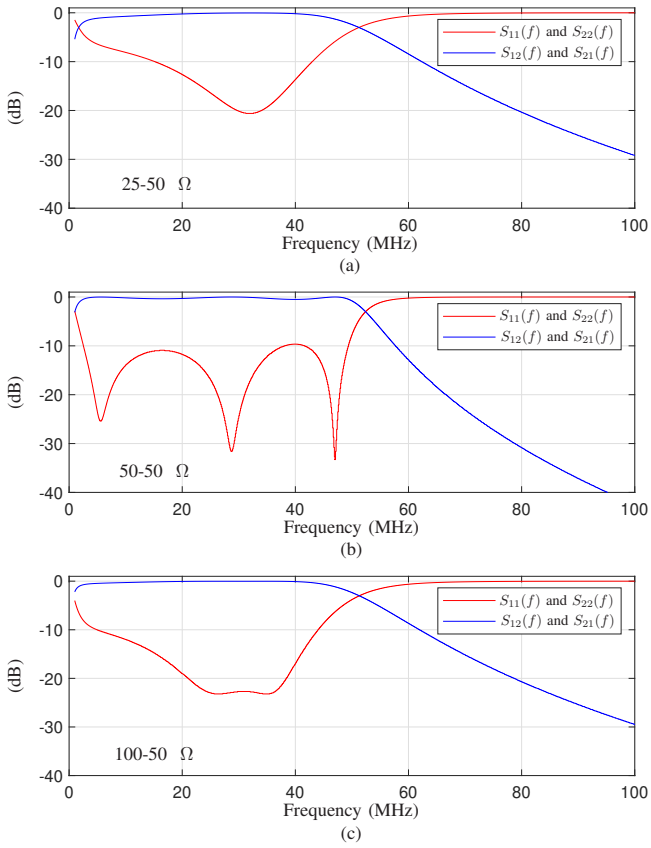

Fig. 4: Magnitude of the scattering parameter $S_{11}(f)$, $S_{22}(f)$, $S_{12}(f)$, and $S_{21}(f)$ of the analog filters designed for the adaptive PLC coupling circuit and the frequency band of $2-50$ MHz. (a) $25-50$ Ω, (b) $50-50$ Ω and (c) $100-50$ Ω.

VI. Conclusion

This paper has proposed an adaptive PLC coupling circuit for the frequency band $2-50$ MHz in order to enhance the impedance matching between PLC transceivers and electric power grids. Based on simulating results, we have shown that the impedance matching between PLC transceivers and electric power grids by using the proposed analog filter bank approach is possible. Indeed, the scattering parameters $S_{11}(f)$ and $S_{12}(f)$ results have shown a satisfactory magnitude in the band-pass, i.e., a low return loss and a high insertion gain. Overall, the filter bank approach seems to be an interesting direction for improving the impedance matching between PLC transceivers and electric power grids.

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